CMOS Image sensor and Image capture on FPGA with master (DMA) transfers

rene.beuchat@epfl.ch
LAP-EPFL
rene.beuchat@hesge.ch
LSN-EIG-HESSO

Objectives

- Examples of CMOS Image sensor
- Internal architecture
- Some characteristics
- Transformations of pictures
- **Master Programmable interface design on Avalon** → to analyze and realize

- **CMOS Sensors :**
  - ➢ Integrated, low-power devices with high image quality.
- Interline CCD :
  - ➢ Progressive scan sensors with electronic shutter for real-time imaging.
- Full Frame CCD
  - ➢ Low noise, high sensitivity imagers for a variety of applications.
- Linear CCD:
  - ➢ High performance monochrome and trilinear (RGB) arrays.

- Example :
  - Kodak Family Image Sensor
    - National Semiconductor → Kodak transfer
  - Low cost
  - N/B or color
  - 128 x 101 (580 frames/s)
  - → 2592 x 1944 pixels (6 frames/s)

CMOS sensor outline

- One case study
- General Camera sensor architecture
- Sensor interface
- Sensor control (i2c)
- Architecture of a Camera controller

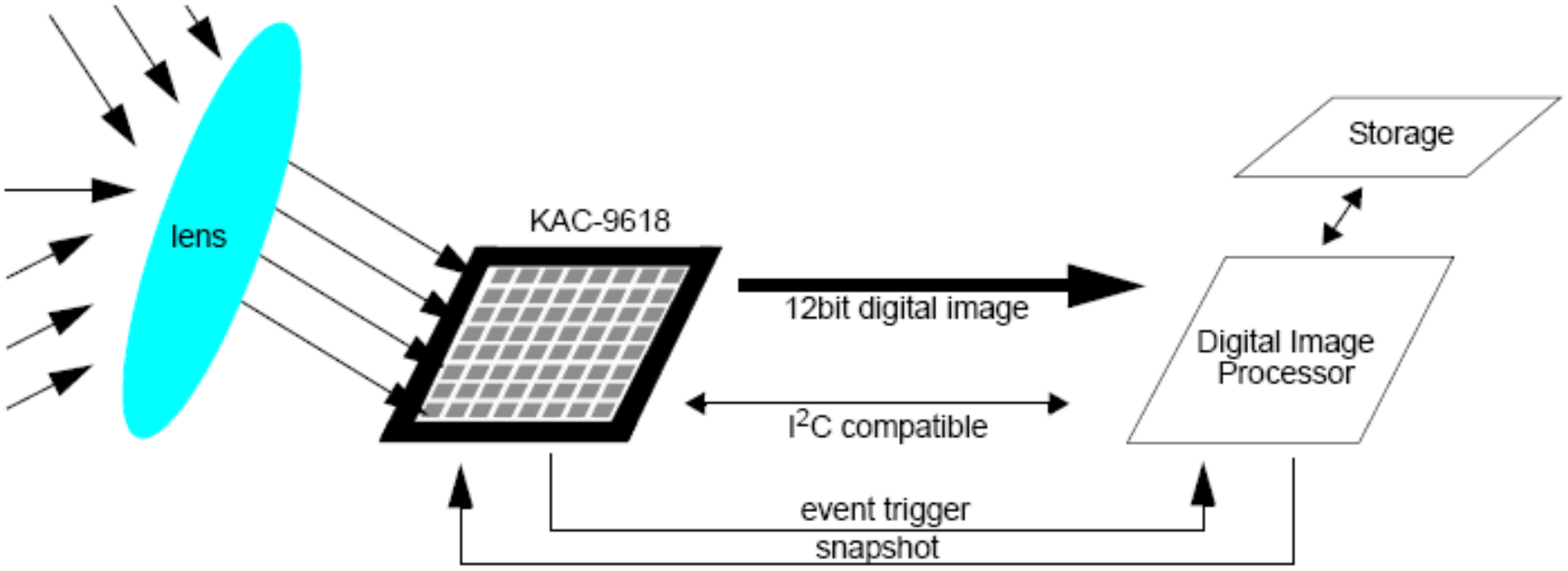
- Other interfaces

CMOS Image sensors (ex. Kodak Family, 2006, discontinuing products)

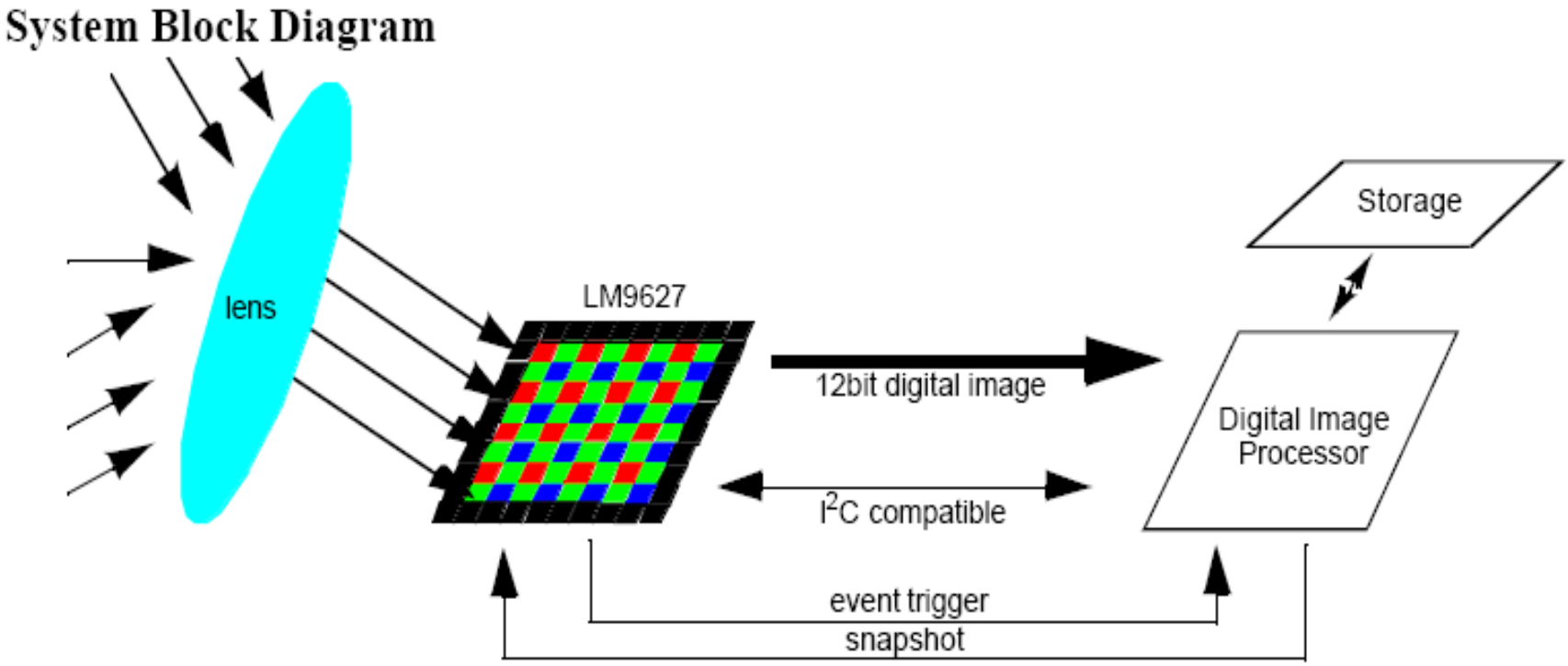
CMOS Image Sensors Device	Resolution	Pixel	µm	Lens Format	Frame Rate (fps)
KAC-9618	VGA	648 x 488	7.5	1/3"	30
KAC-9619	VGA	648 x 488	7.5	1/3"	30
KAC-9628	VGA	648 x 488	7.5	1/3"	30
KAC-00400	WVGA	768 x 488	6.7	1/3"	60
KAC-01301	1.3 MP	1284 x 1028	2.7	1/4"	15
KAC-3100	3.1 MP	2048 x 1536	2.7	1/2.7"	10
KAC-5000	5.0 MP	2592 x 1944	2.7	1/1.8"	6

- Today (2009) max resolution is about
- **50 Mpixels** commercially available

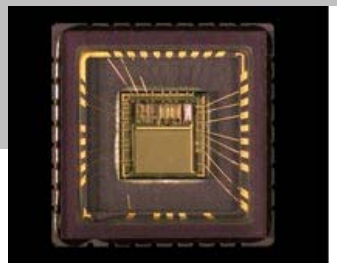
BW CMOS sensor



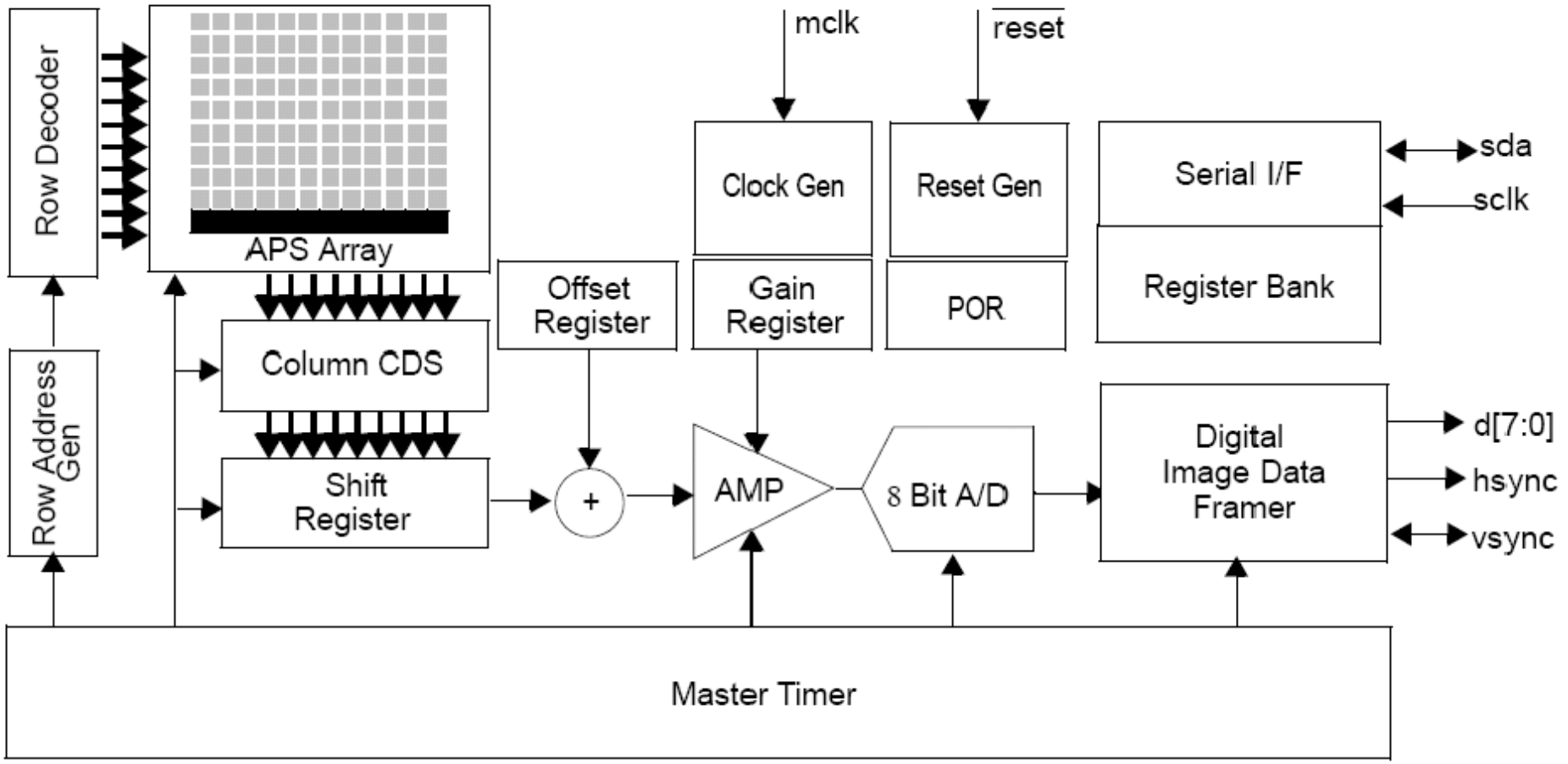
System Architecture



LM9630, B/W

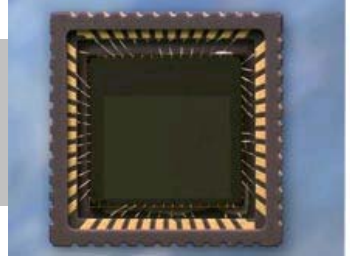


Internal Architecture



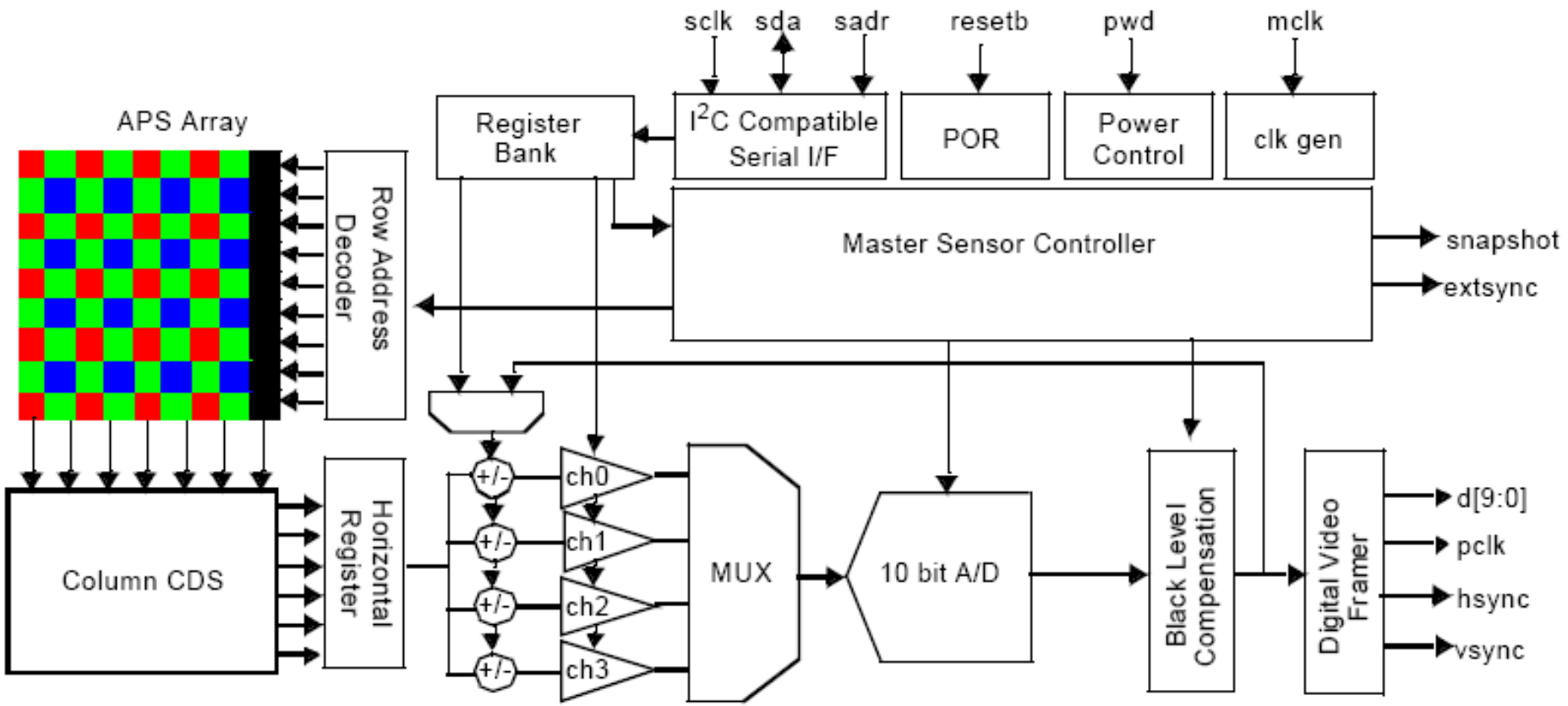
http://www.kodak.com/ezpres/business/ccd/global/plugins/acrobat/en/datasheet/cmos/KAC-9630LongSpec.pdf

LM9638, color

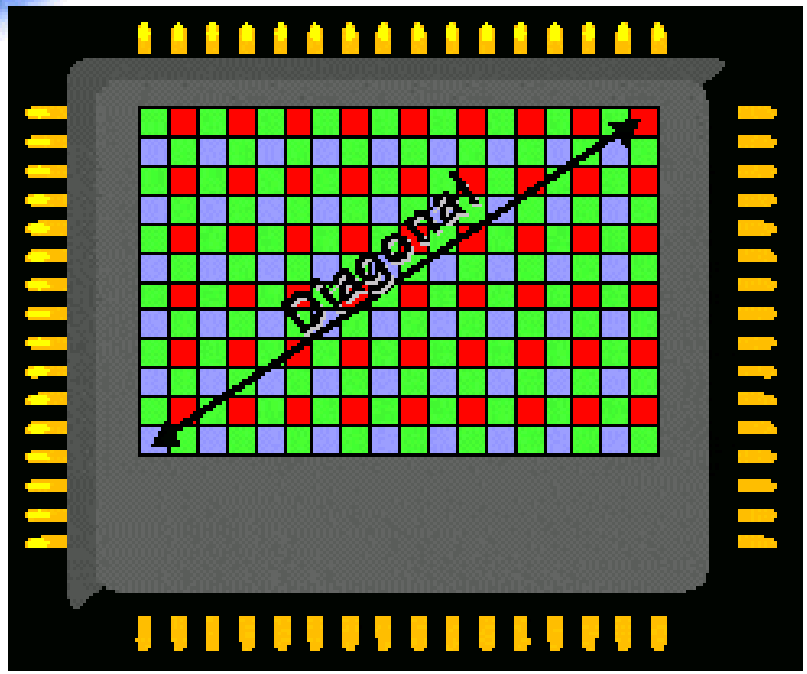


Internal Architecture

Overall Chip Block Diagram



Pixel Array

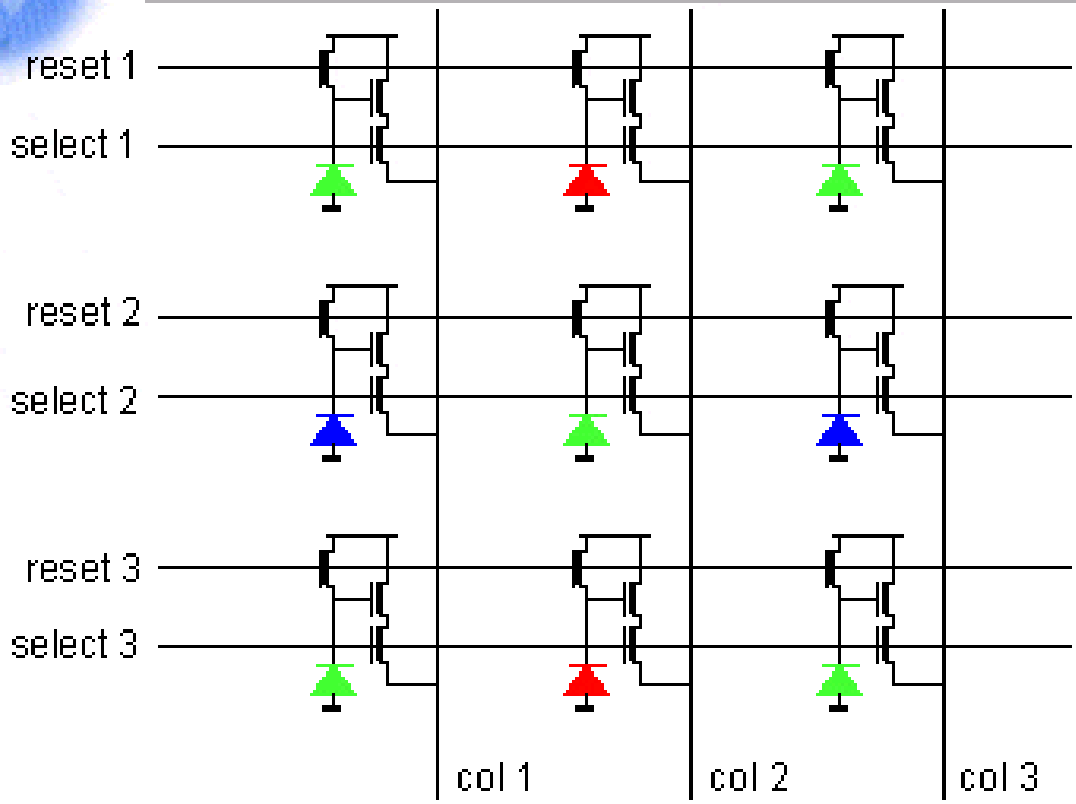


Resolution: number of column and Rows in the array e.g. VGA 640*480
Pixel Pitch: The size of each pixel e.g. 7.5 µm * 7.5 µm
Diagonal: Determines the Lens size e.g. 1/3" Lens.
Active Pixels: Pixels that can be used to detect light.
Black Pixels: Optically shielded pixels used as a reference for black level.

A CMOS image sensor consists of a two dimensional array of picture elements (pixels). In a color sensor the pixels are covered by color filters.

National Semiconductor
The Sight & Sound of Information

The Array



A CMOS array has reset, select, and column readout lines across its surface. The pixel consists of a photodiode and transistors.

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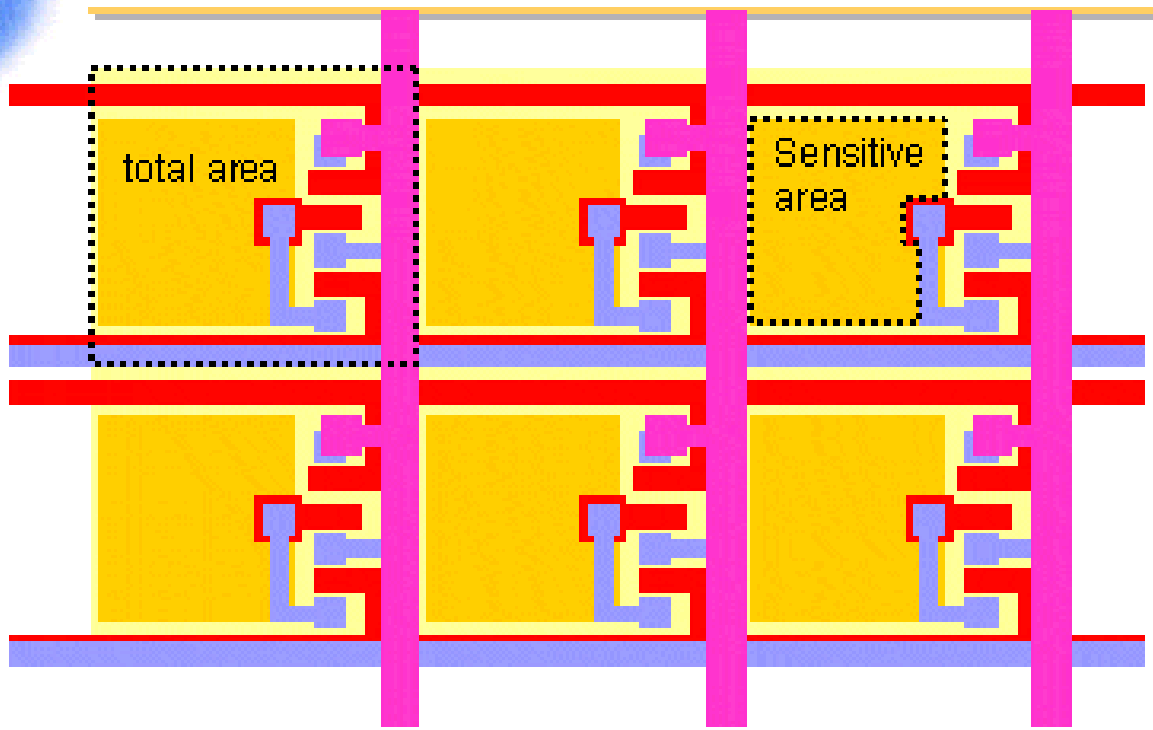
Fill Factor



Fill factor = sensitive area / total area

The fill factor (area efficiency) of the array is the probability that an incident photon will enter the light sensitive area (photodiode) instead of the wires and transistors.

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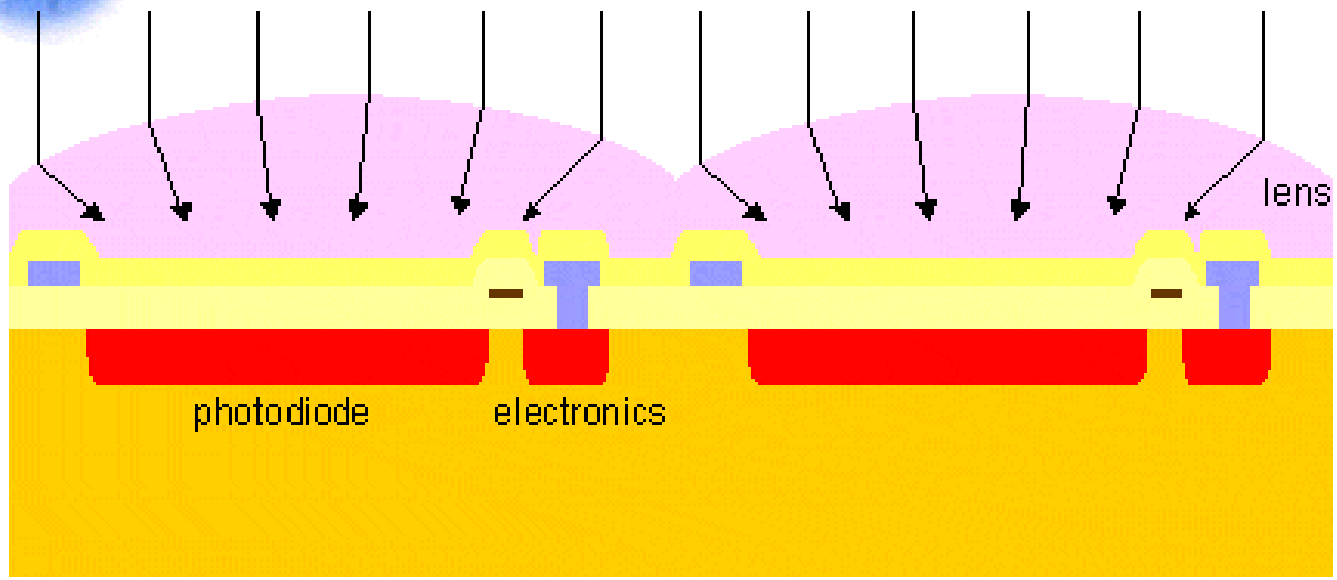
Micro Lenses



The fill factor can be improved using micro lenses on the surface of the image sensor. The micro lenses focus the light on the sensitive area.

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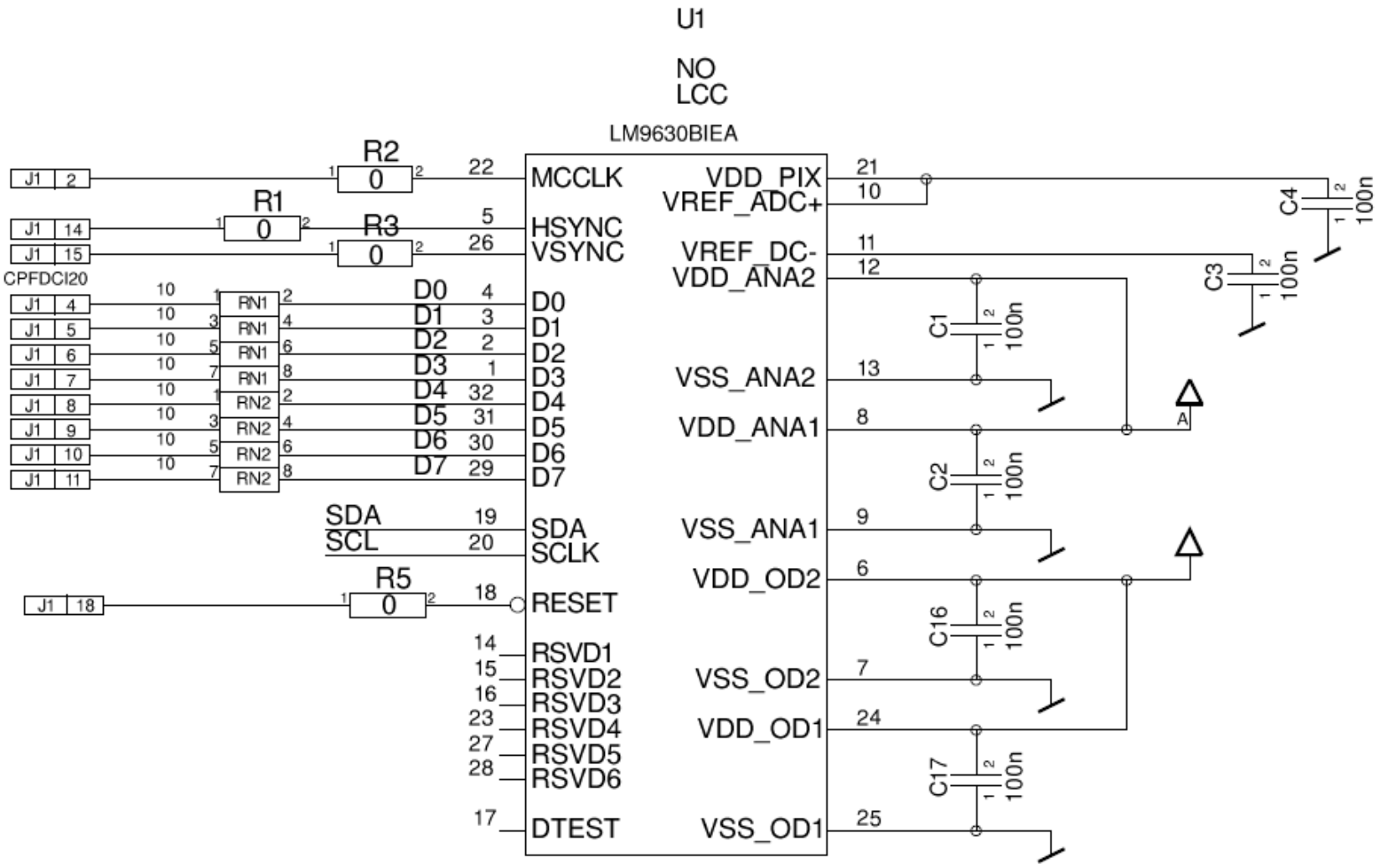
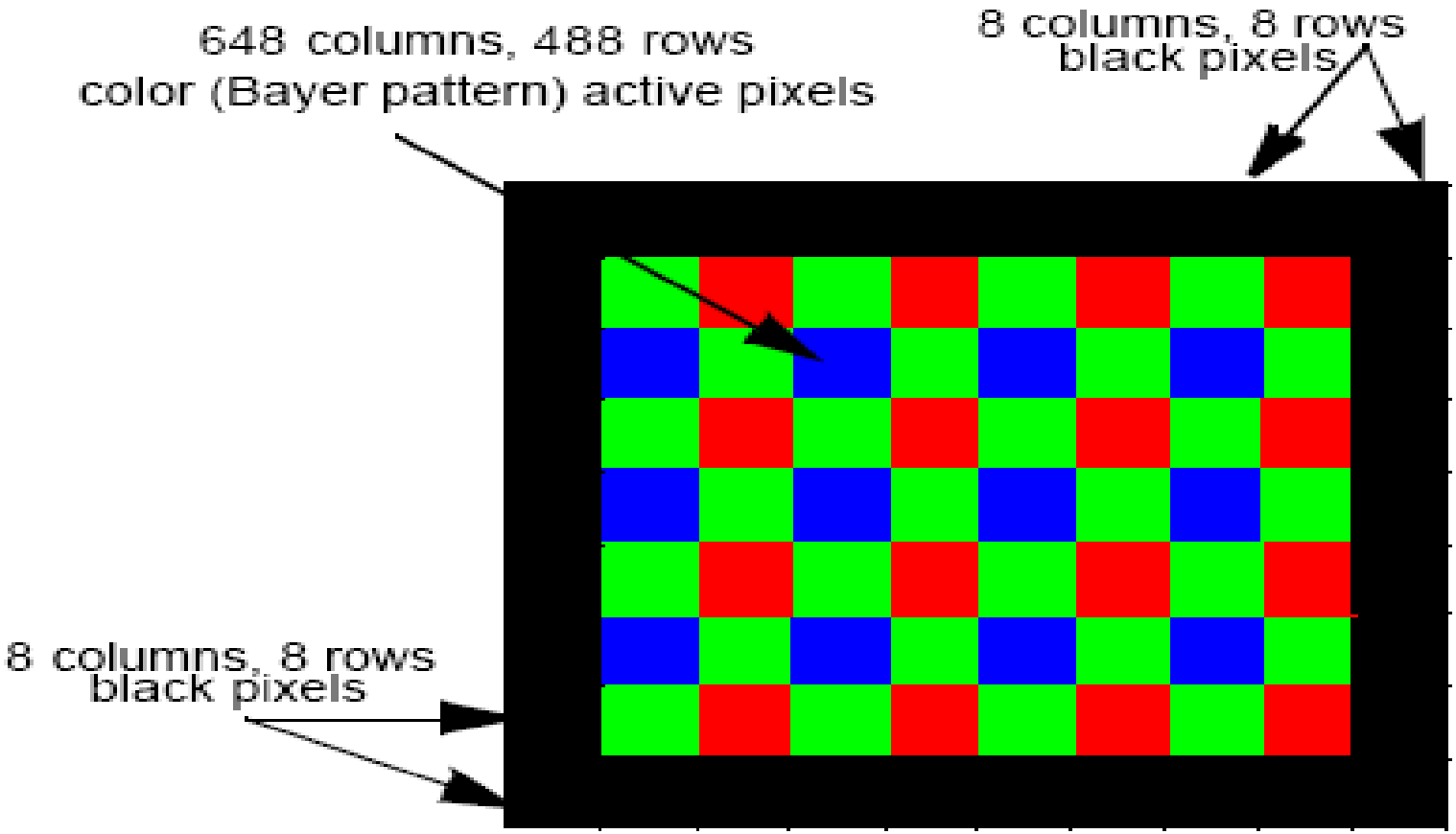
LM9630 main characteristics

Array Format	
Total	128H x 101V
Active	118H x 96V
Effective Image Area	
Total	2.56 mm x 2.00 mm
Active	2.36 mm x 1.92 mm
Optical Format	1/5"
Pixel Size	20µm x 20µm
Video Outputs	8 Bit Digital
Frame Rate	580 frames per second
Dynamic Range	48 dB
Electronic Shutter	Global Reset

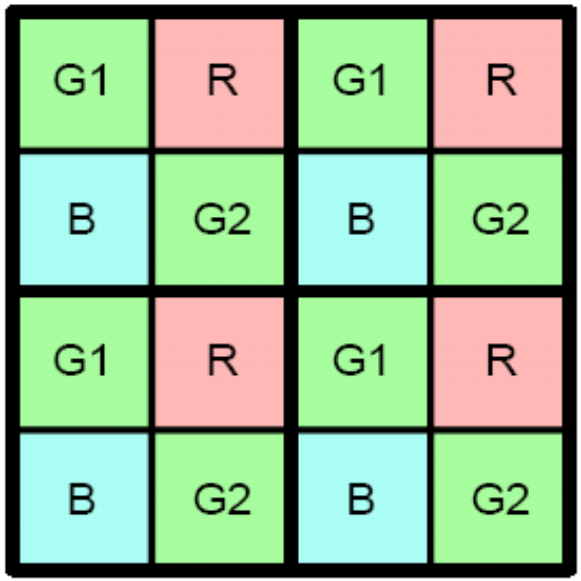
Module 9630, 20 pins connector

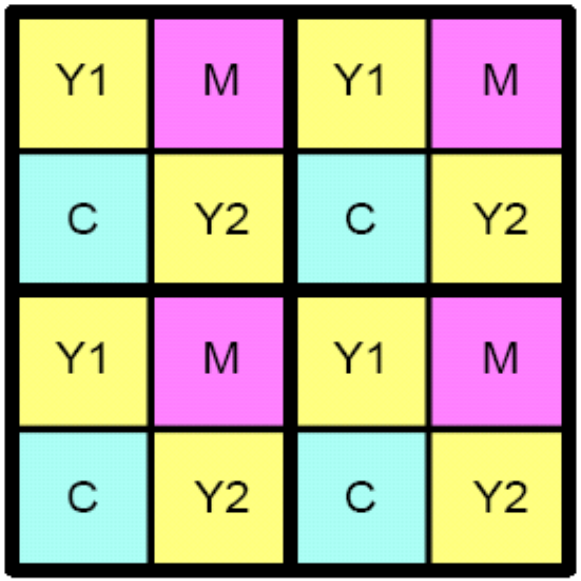


Color Mosaic, Bayer pattern, 1 color/pixel



Color Mosaic



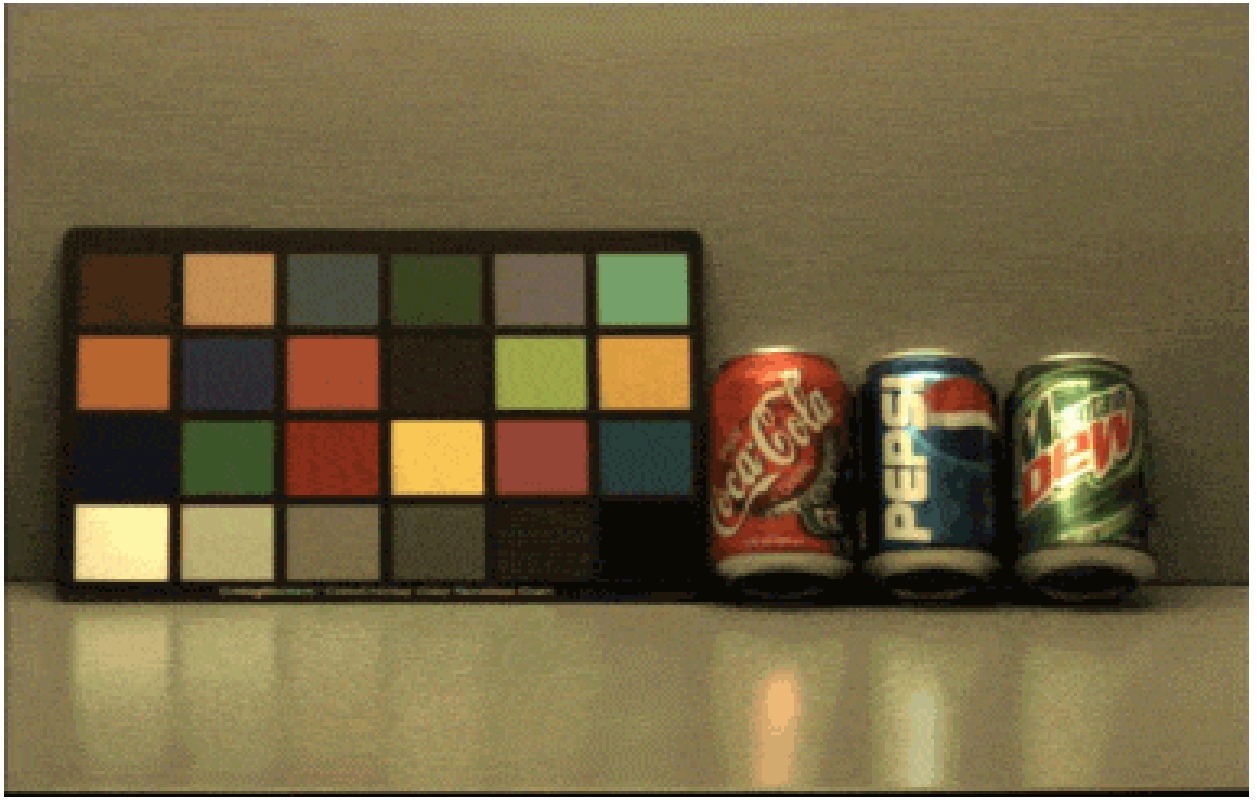


Red Green Blue Bayer Pattern

Yellow Magenta Cyan Bayer Pattern

http://www.kodak.com/ezpres/business/ccd/global/plugins/acrobat/en/supportdocs/ColorCorrectionforImageSensors.pdf

Color Interpolation



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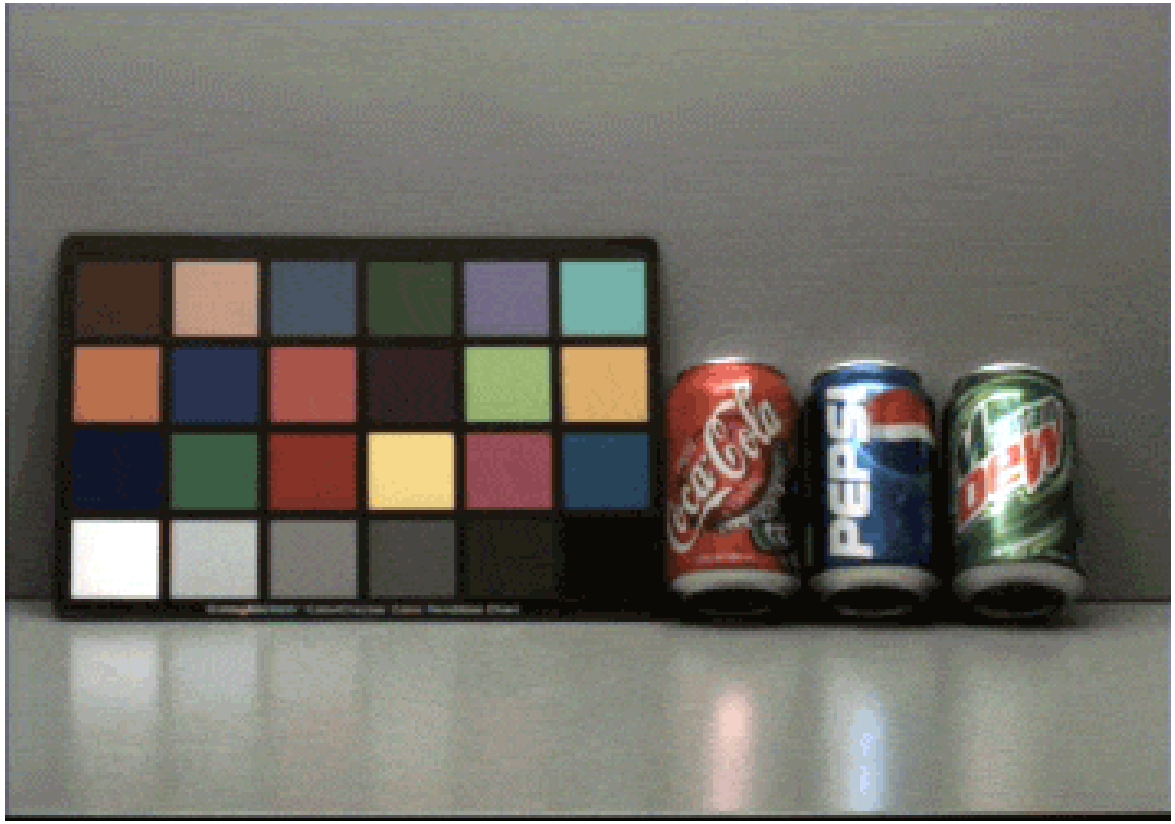
White Balance



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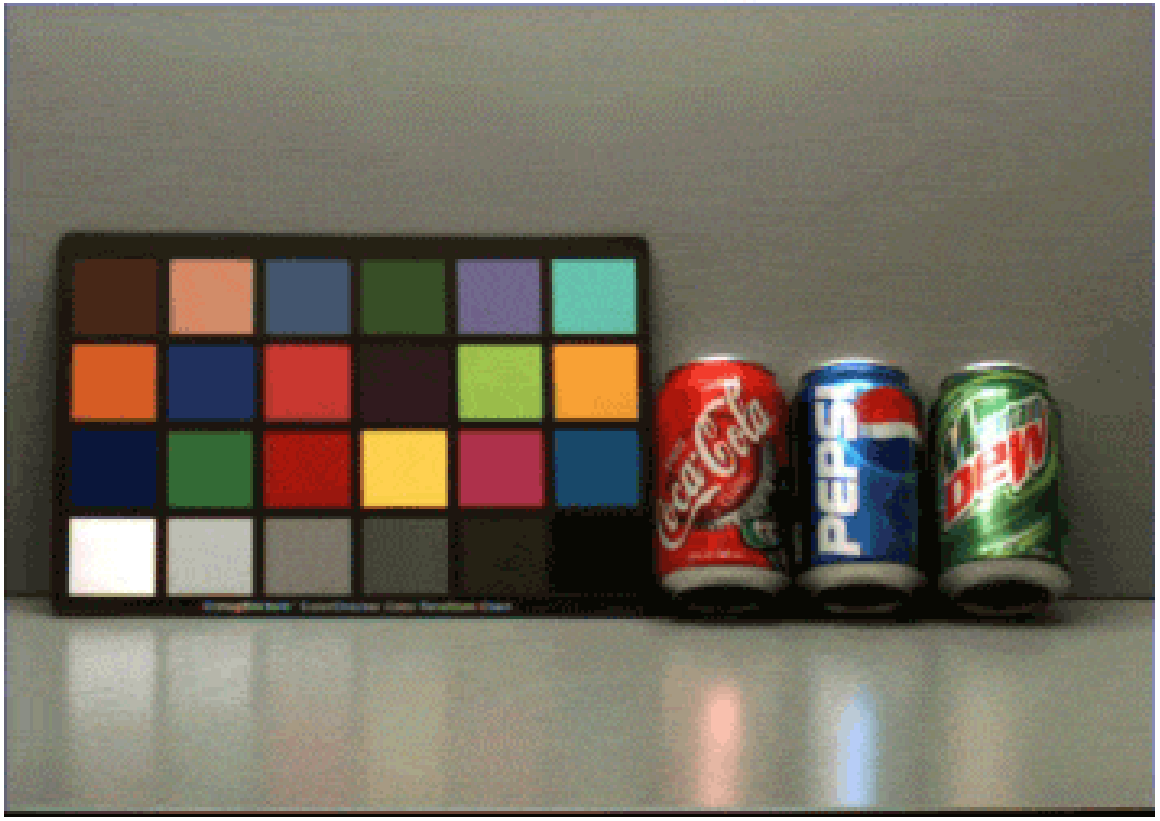
Color Correction



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Gamma Correction

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Edge Enhancement

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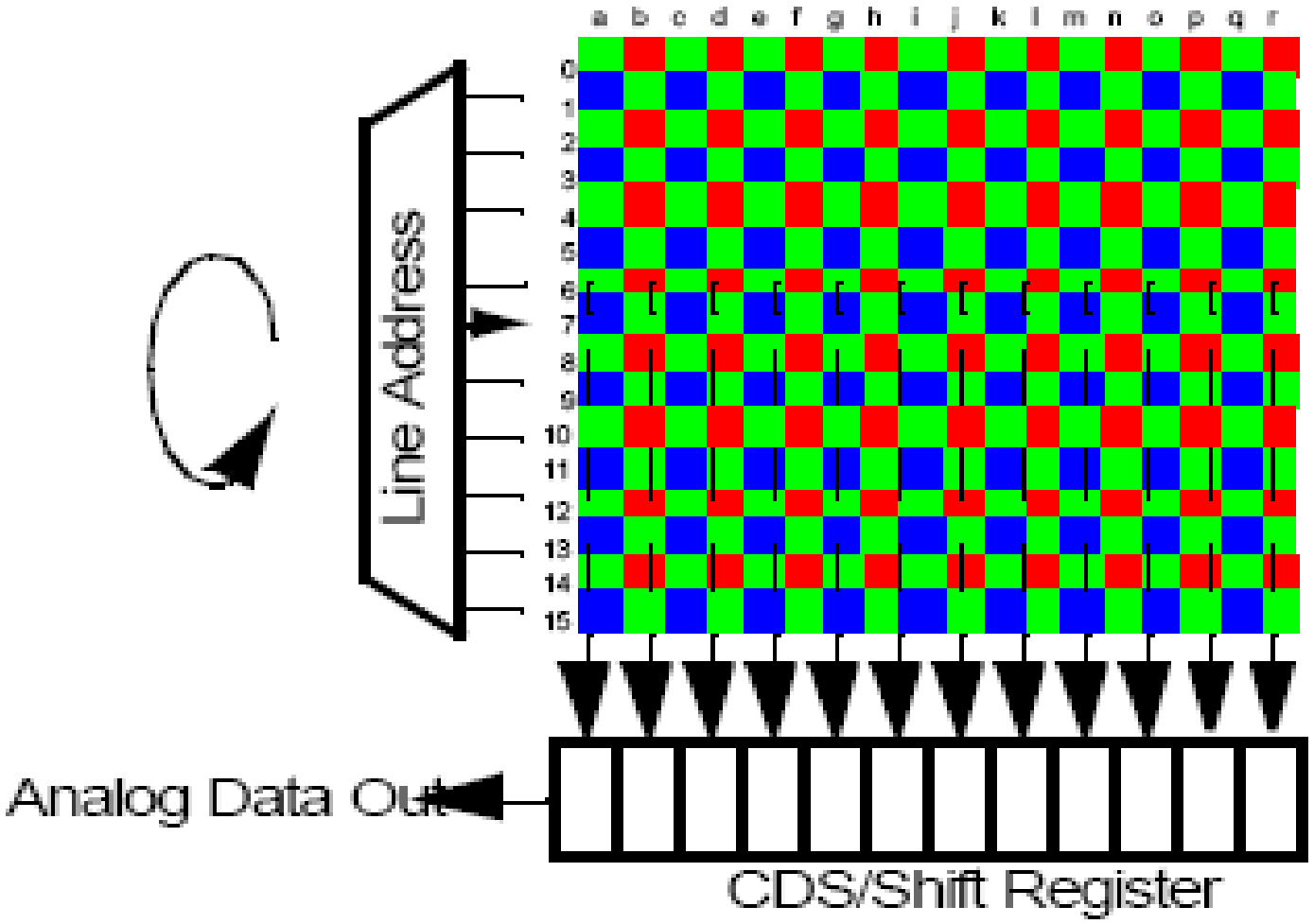
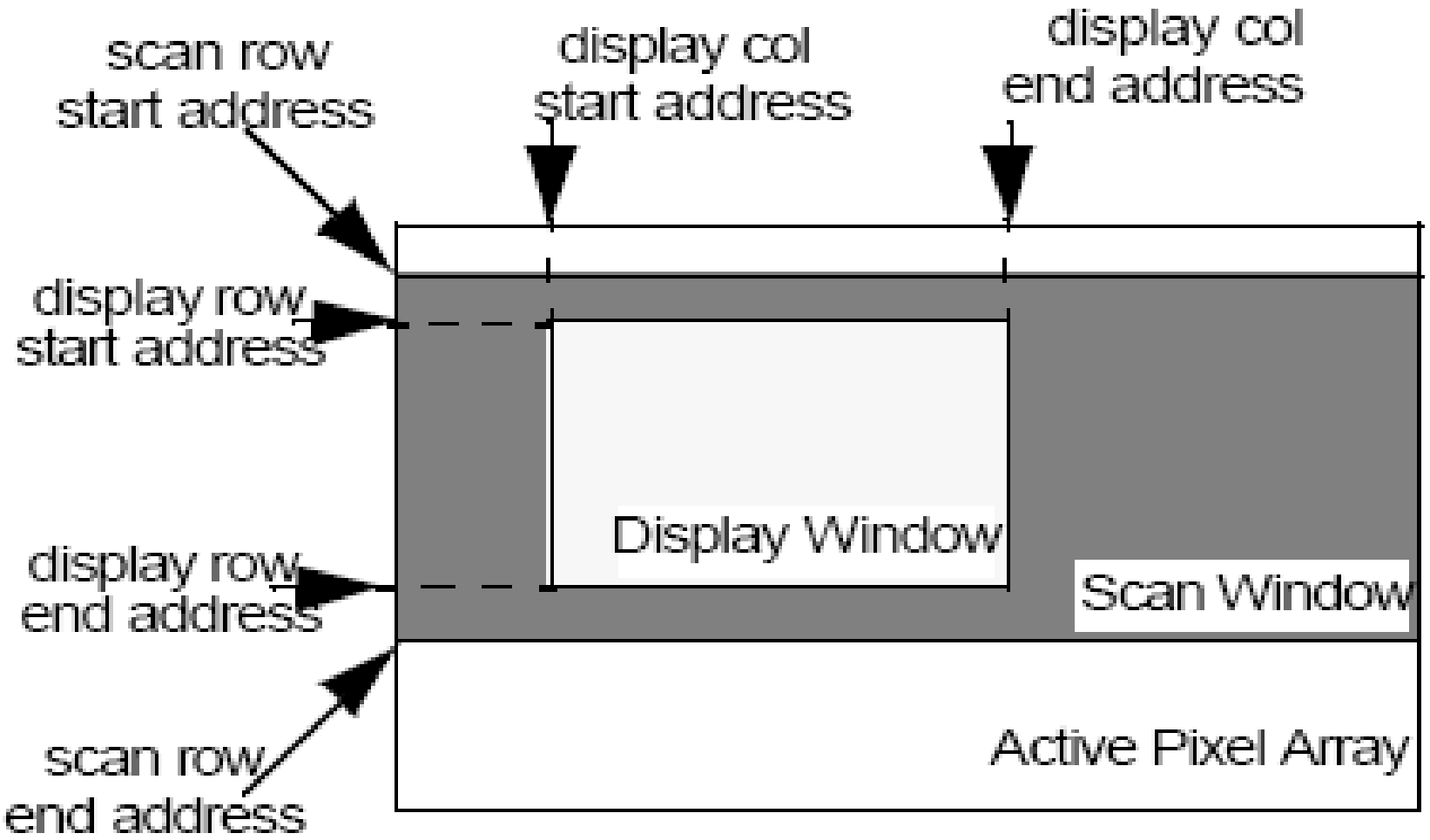
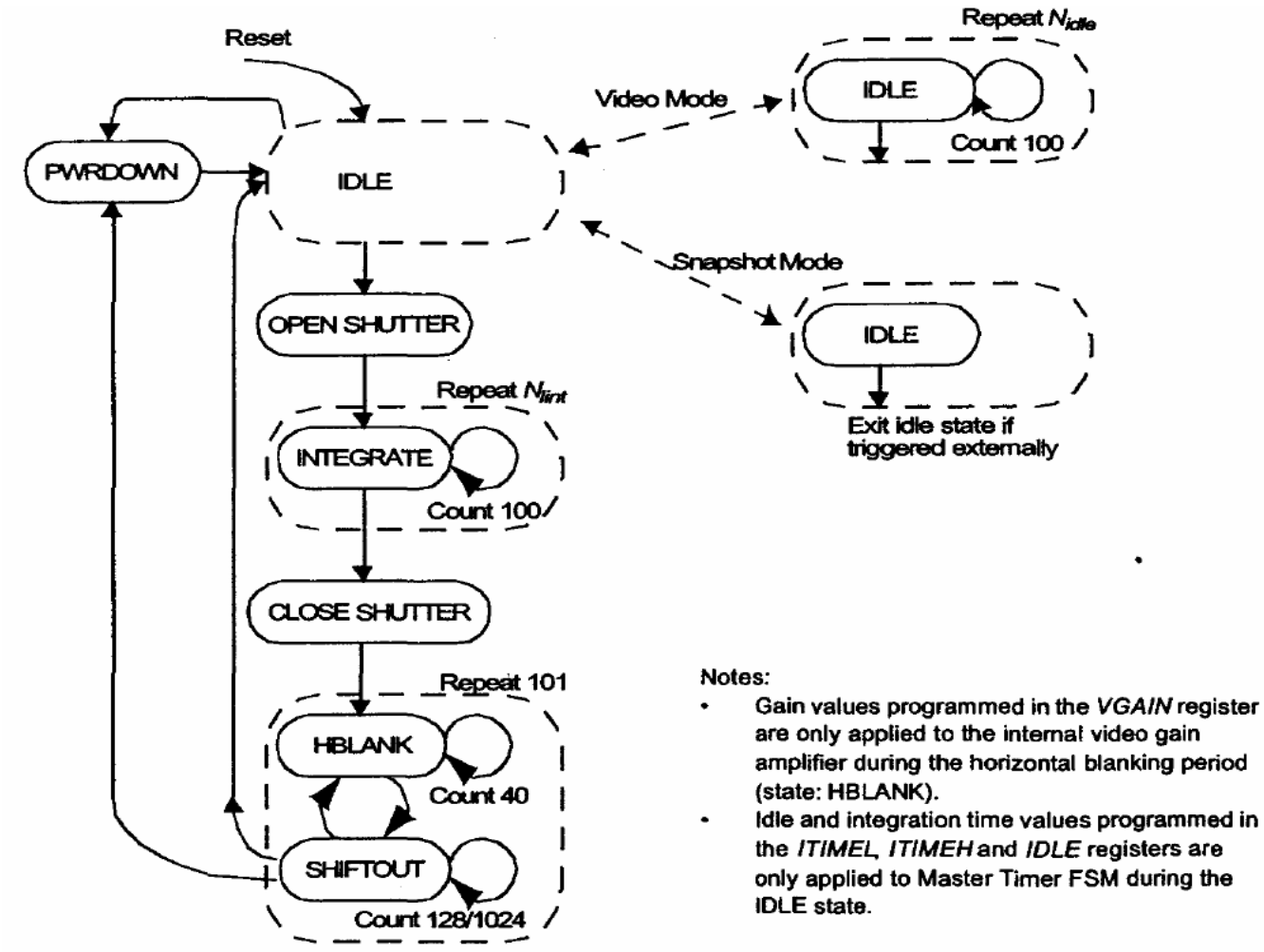
Row scanning



Windowing


scan row
start address
display col
start address
display col
end address
display row
start address
Display Window
display row
end address
Scan Window
scan row
end address
Active Pixel Array

Sensor Reading



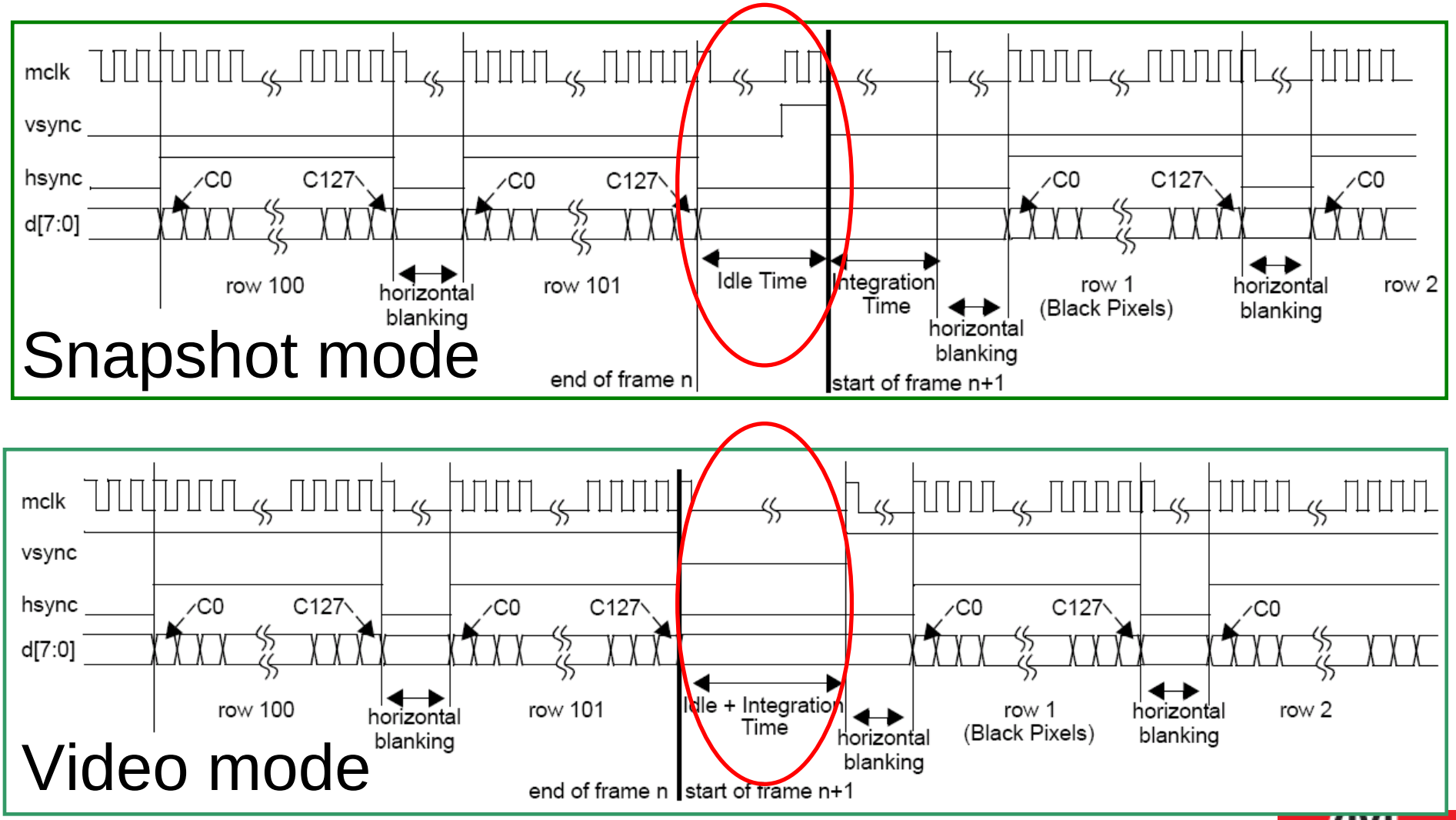
Notes:

- Gain values programmed in the *VGAIN* register are only applied to the internal video gain amplifier during the horizontal blanking period (state: HBLANK).
- Idle and integration time values programmed in the *ITIMEL*, *ITIMEH* and *IDLE* registers are only applied to Master Timer FSM during the IDLE state.

Exemple with KAC-9630 (Kodac, obsolete now)

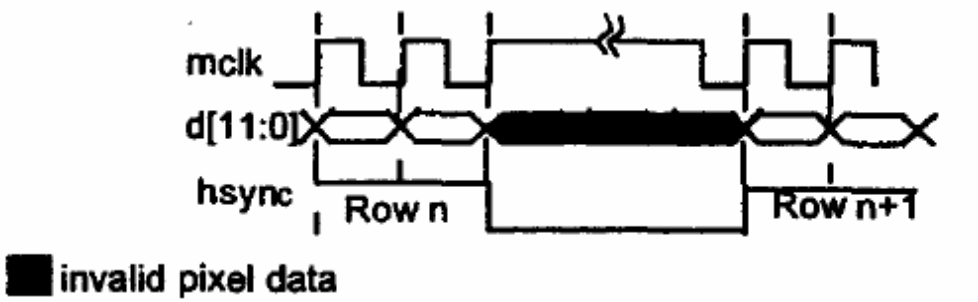
http://www.kodak.com/global/en/business/ISS/Products/CMOS/KAC-9630/support.jhtml

Video signals

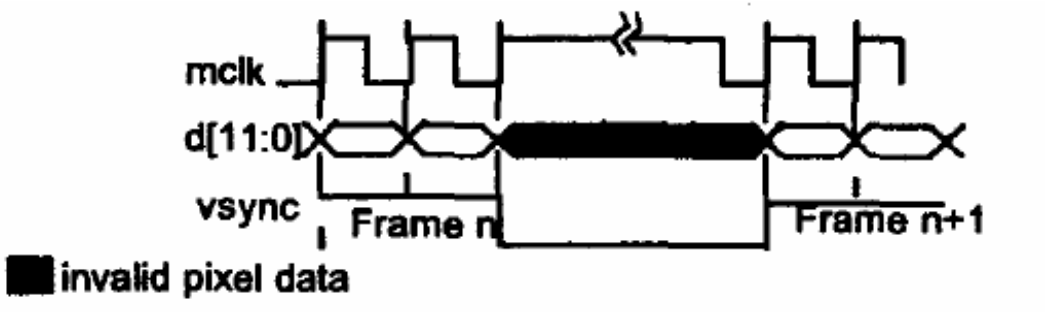


Video signals

- In snapshot mode, the VSync need to be at least **2 MClk** wide. When deactivated, the integration time programmed in ITIMEx start



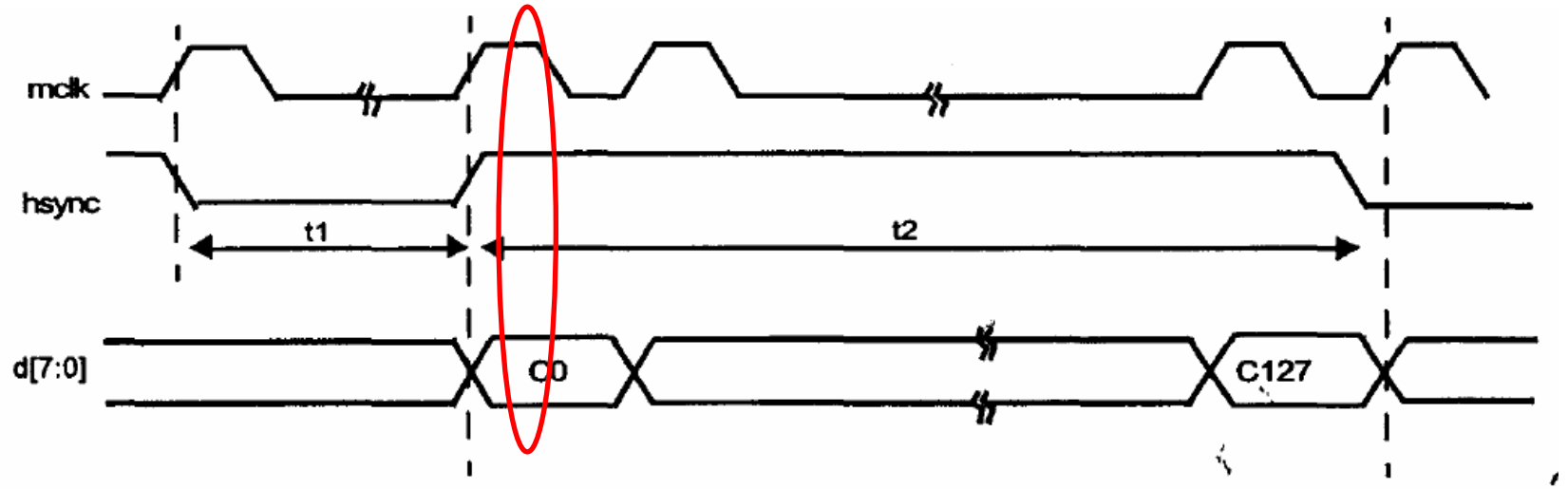
- *Relations between HSync, Mclk, and pixels*



- *Relations between VSync, Mclk, and pixels*

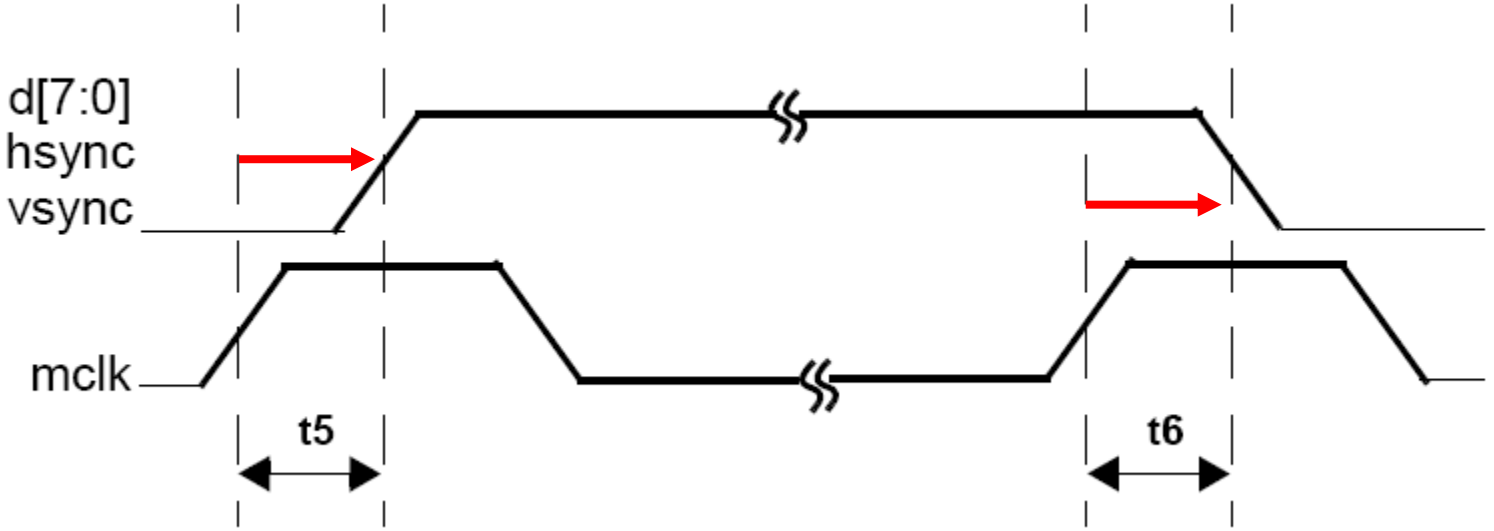
Video signals

- All signals are synchronized on the MClk input signal.



- *Relation Mclk, HSync, Data*
- t1 = 40 * mclk → idle time between two rows
- t2 = 128 * mclk → number of pixels on a row

Video signals



- *t5, t6 : 10-25ns*
- → t5 & t6 are the delay between rising edge of Mclk and other signals

Video signals

- The **idle** time **Nidle<10..0>** is:
- In video mode: programmable in the registers **ITIMEH:<5..3>** and **IDLE<7..0>** by step of **100 * Mclk**. The value is to be written in 2 registers as Nidle<10..0> value on 11 bits. The minimum value is 1, max 0x7FF, 100 Mclk .. 204'700 Mclk → 10 µs ... 2.047 ms for a 10MHz Mclk.
- In snapshot mode, it will depend on the VSync pulse external activation

Internal registers transfer by i2c

ADDR	Register	Reset Value	Description
00h	REV	00h	Silicon Revision & Bank Enable Register
01h	MCFG	00h	Main Configuration Register.
02h	VGAIN	00h	Video Gain Register
03h	ITIMEL	0Ah	Integration Time Low Register
04h	IDLE	00h	Idle Time Register
05h	ITIMEH	00h	Integration Time High Register
06h	POWSET		Power Setting Register
07h			Reserved
08h	OFFSET	00h	Offset Adjustment Register

Configuration by i²c

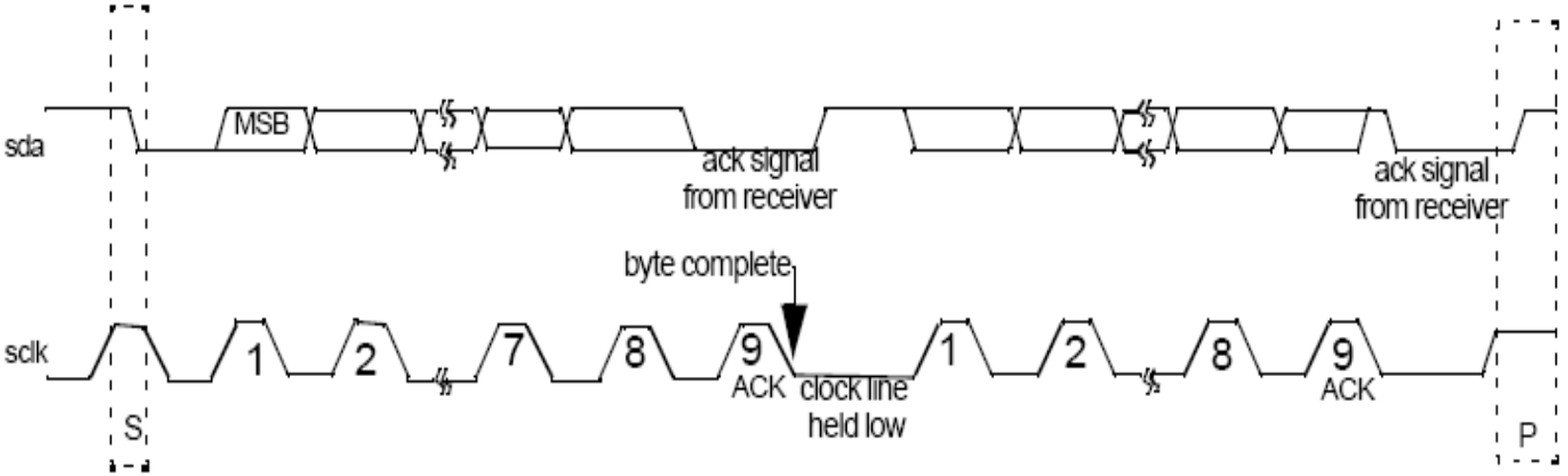


Figure 30. Serial Bus Byte Format

bold **sensor action**

Figure 31. Serial Bus Write Operation

bold **sensor action**

Design of a Camera Controller

- Design on a FPGA
- Camera sensor interface
- Frame grabber

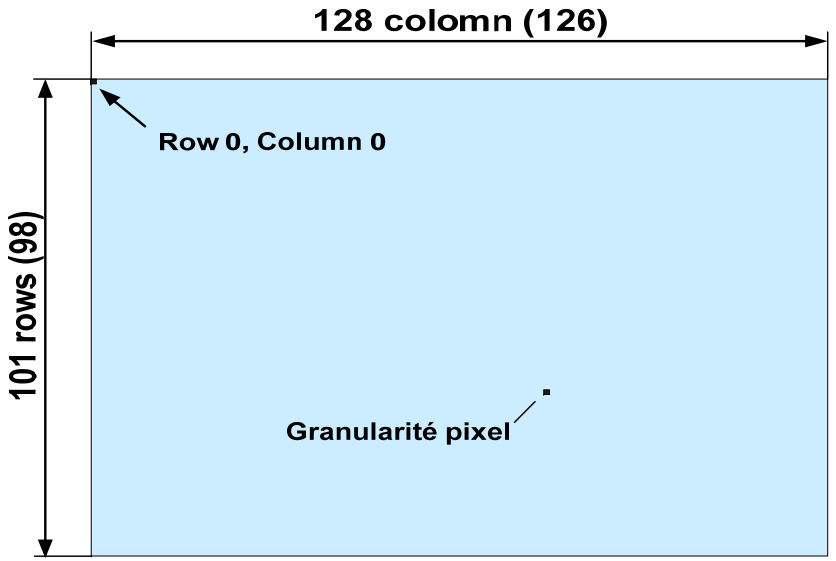
Design of a Camera Controller

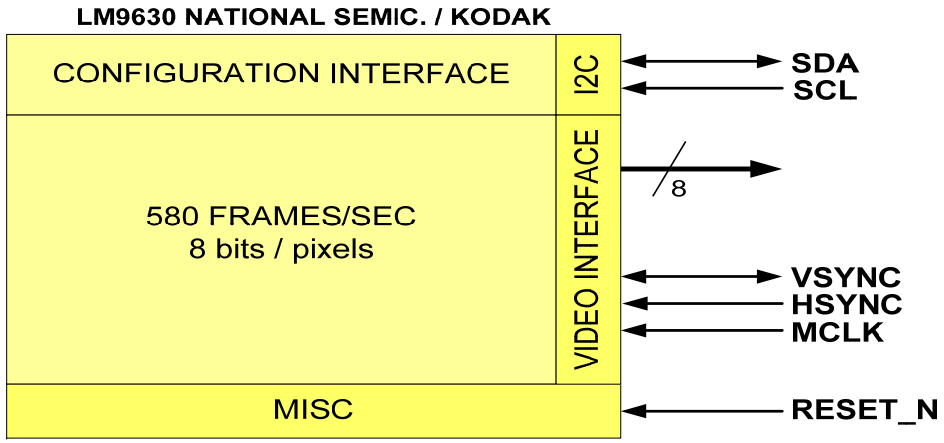
- Module for development on FPGA, 20 pins connector:
  - Cyclone Robot
  - FPGA4U

External interfaces – *camera*

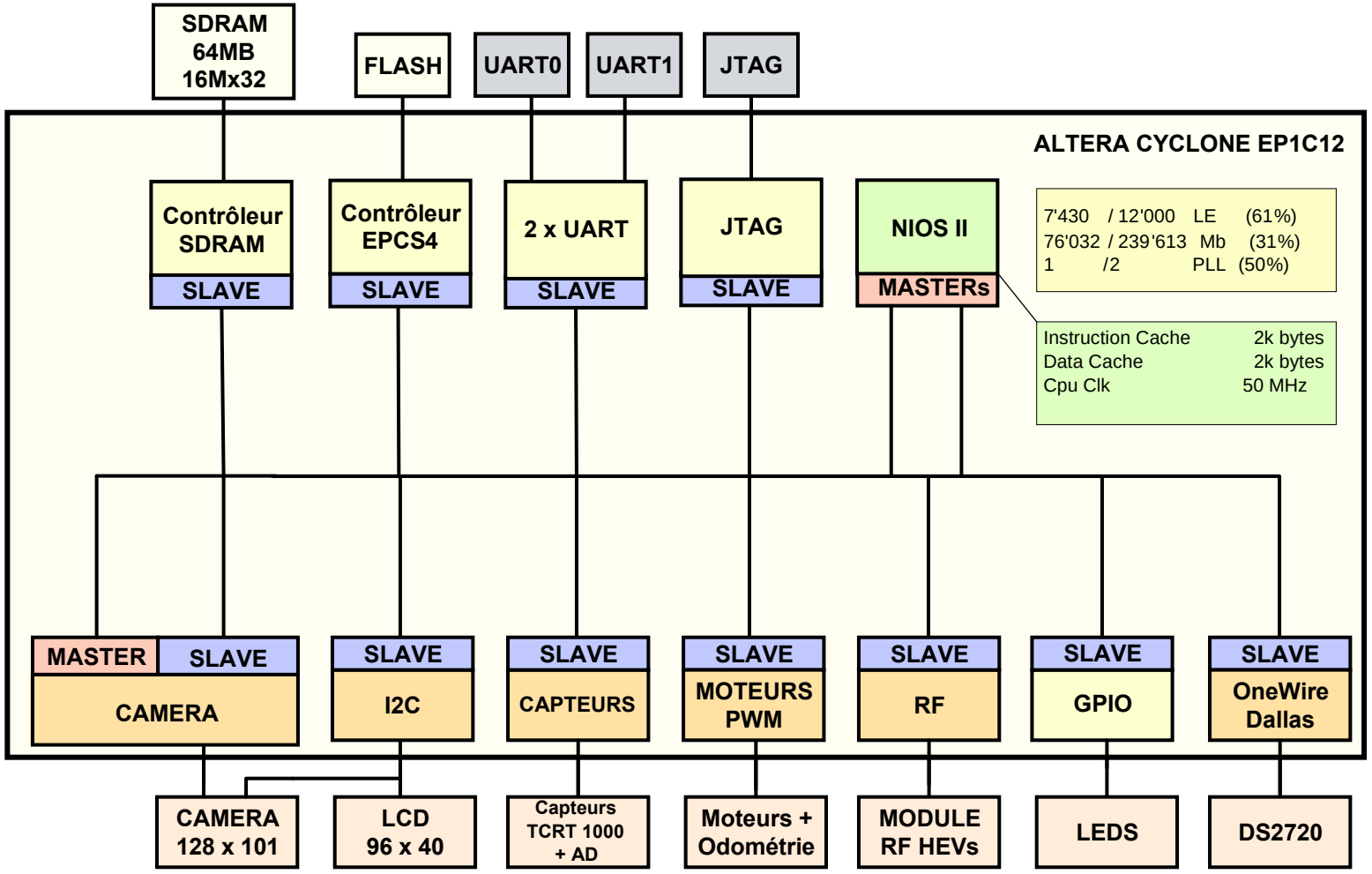
CMOS Camera

KAC-9630 (LM9630)



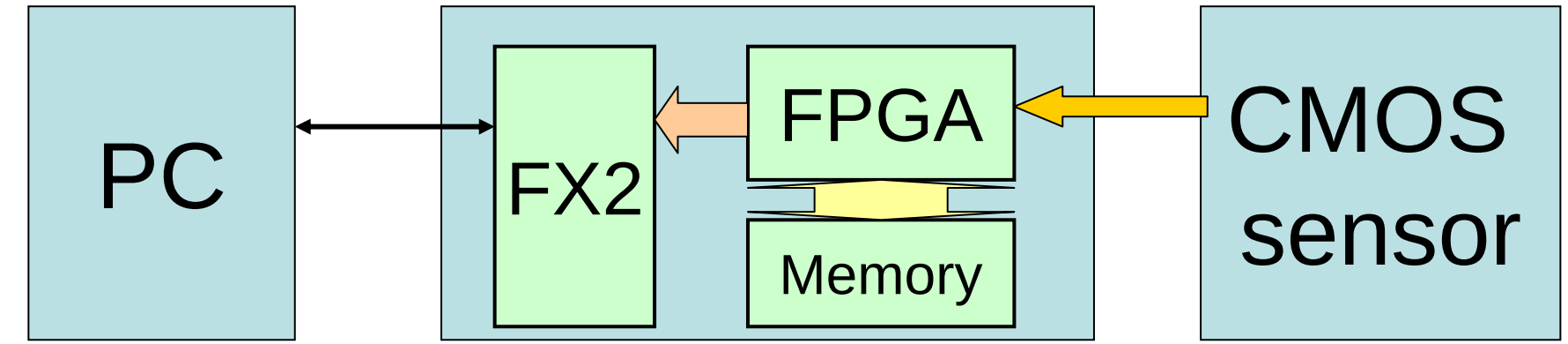


Application – Robot

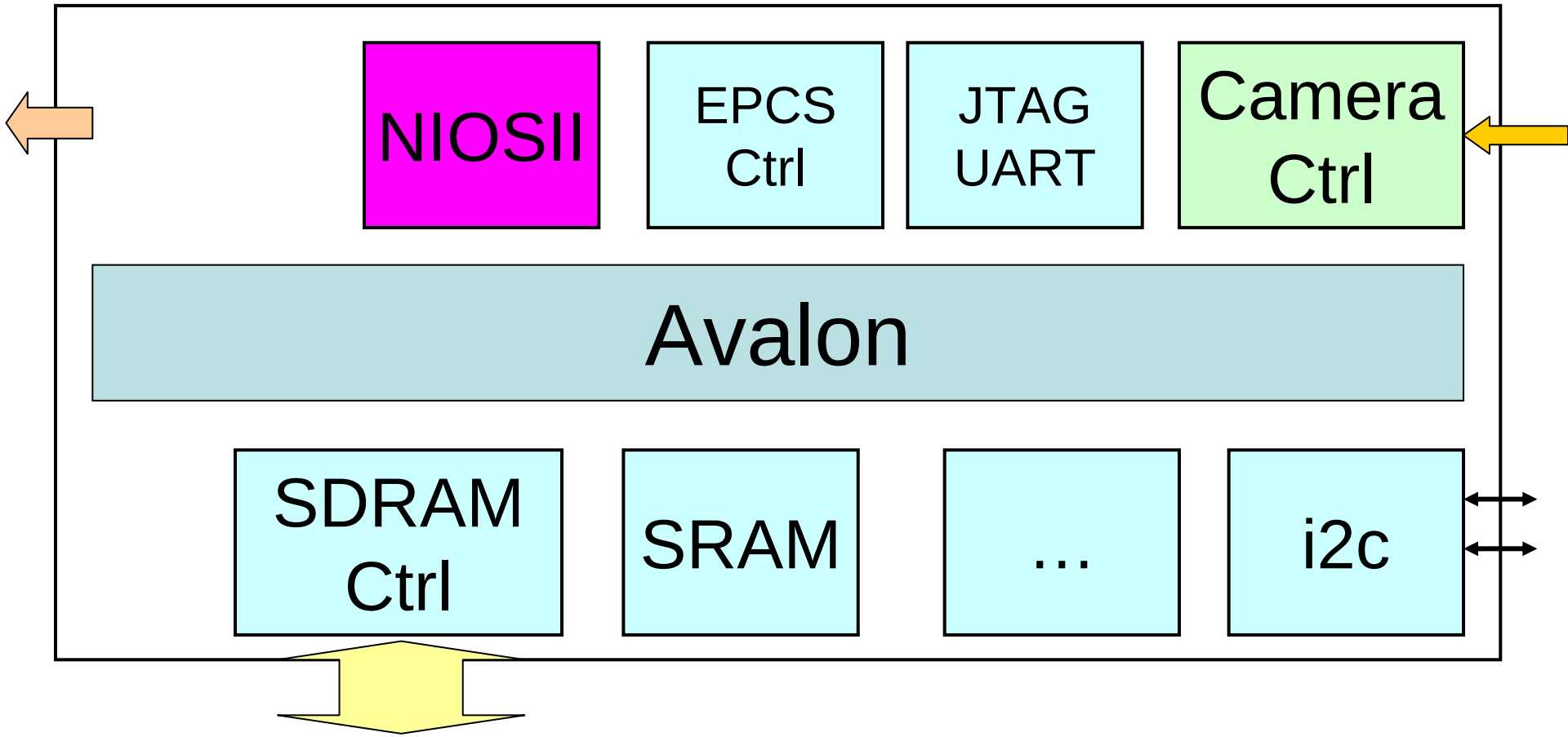


Small camera interface

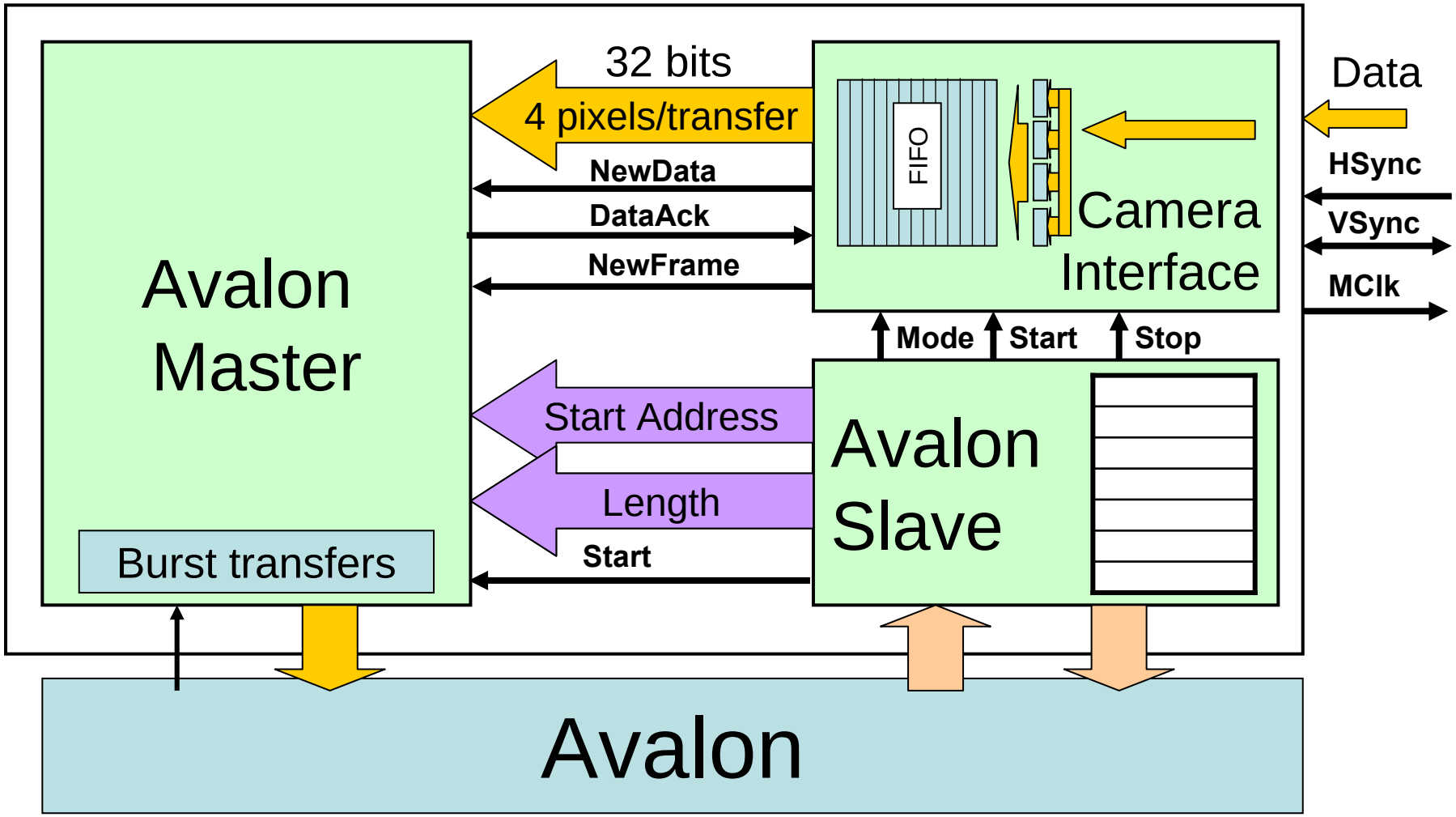
- USB interface to FPGA
  - FPGA for camera control and transfers
  - Sensor → FPGA → Memory
  - Memory → FPGA → USB FIFO (FX2)
  - FX2 → PC



FPGA architecture



Camera Controller architecture



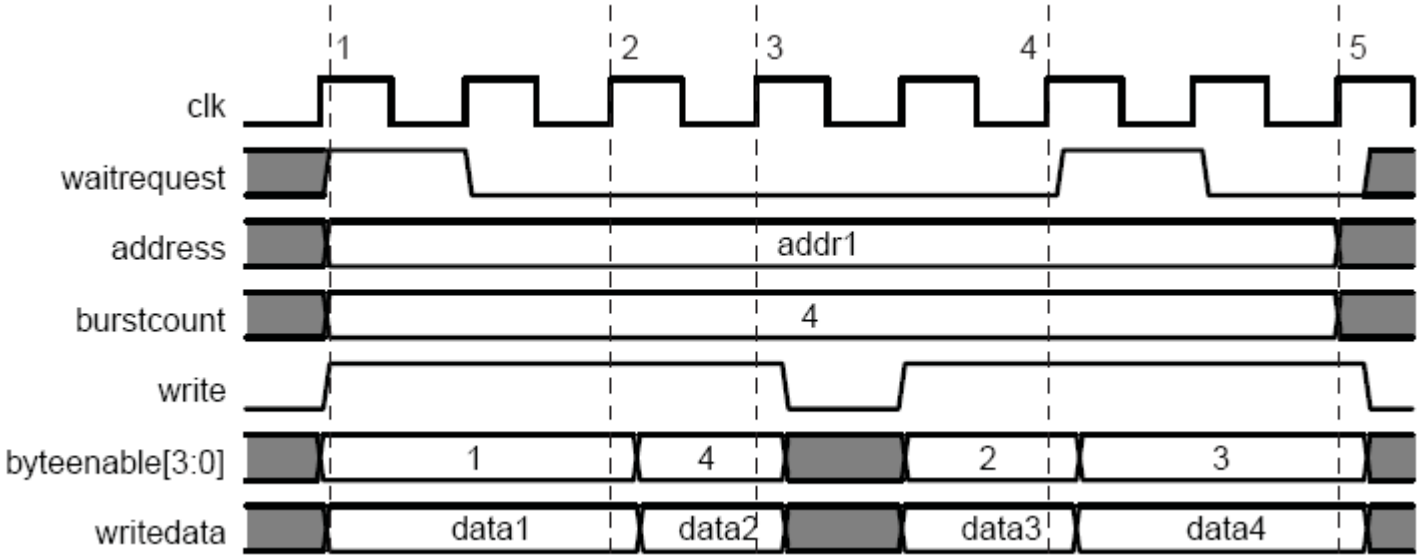
Camera Interface, signals

- Camera interface :
  - Mclk — Cam_Mclk
  - HSync — Cam_HSync
  - VSync — Cam_VSync
  - CamData[7..0] — Cam_data[7..0]
  - CamReset_n — Cam_Reset_n

- Slave interface → interface programmation
  - Clk — Clk
  - Address — AS_Address[2..0]
  - CSelect — AS_Cs_n
  - Write — AS_Write_n
  - DataWrite[31..0] — AS_Datawr[31..0]
  - Read — AS_Read_n
  - DataRead[31..0] — AS_Datard[31..0]
  - InterruptRequest — AS_IRQ_n
- Master interface → Data transfers to memory :
  - Clk — Clk
  - Address [31..0] — AM_Address[31..0]
  - ByteEnable_n[3..0] — AM_ByteEnable_n[3..0]
  - BurstCount — AM_BurstCount[2..0]
  - Write — AM_Write_n
  - DataWrite[31..0] — AM_Datawr[31..0]
  - WaitRequest — AM_WaitRequest

Camera Interface, signals

- As a master, burst access allows the transfer of uninterruptable data flow
- The **BurstCount** is provided by the master unit and the number of announced data has to be provided



Camera Interface, slave access: internal registers

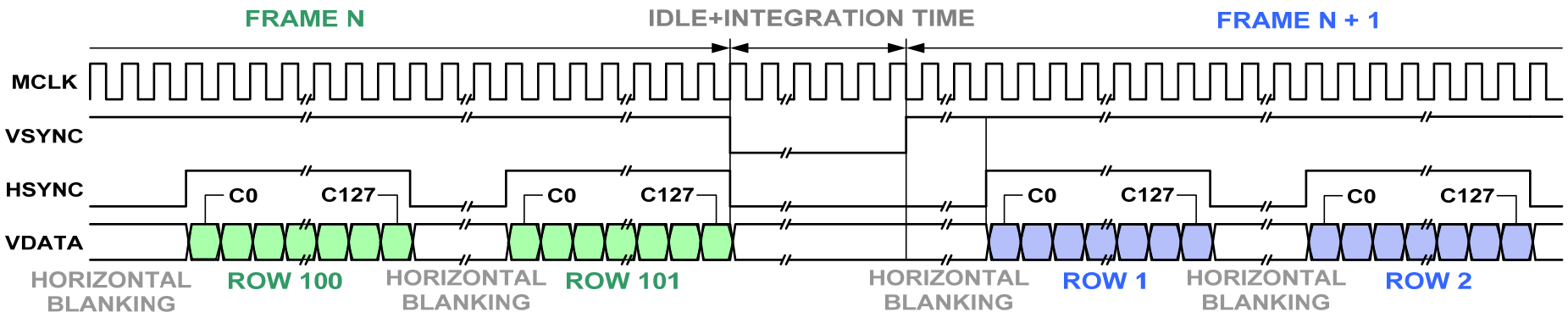
Address	Register	Rz value	Size	Description
00h	**CamAddr**	0h	32	Destination Address
04h	**CamLength**	128*101	24	Buffer size in bytes
08h	**CamComm**	00h	8	Command
0Ch	**CamStatus**	00h	8	Status
10h	**CamStart**	0	8	Acquisition enabled
14h	**CamStop**	0	8	Stop acquisition
18h	**CamSnapshot**	0	8	Snapshot, activate VSync

External interfaces – *camera video signals*

Interface vidéo LM9630

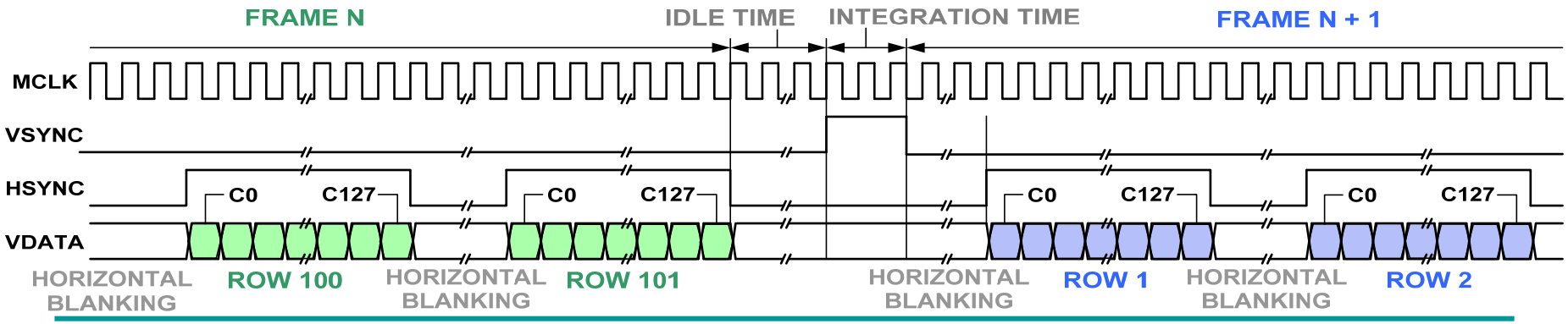
VIDEO MODE

VSYNC = OUTPUT



SNAPSHOT MODE

VSYNC = INPUT



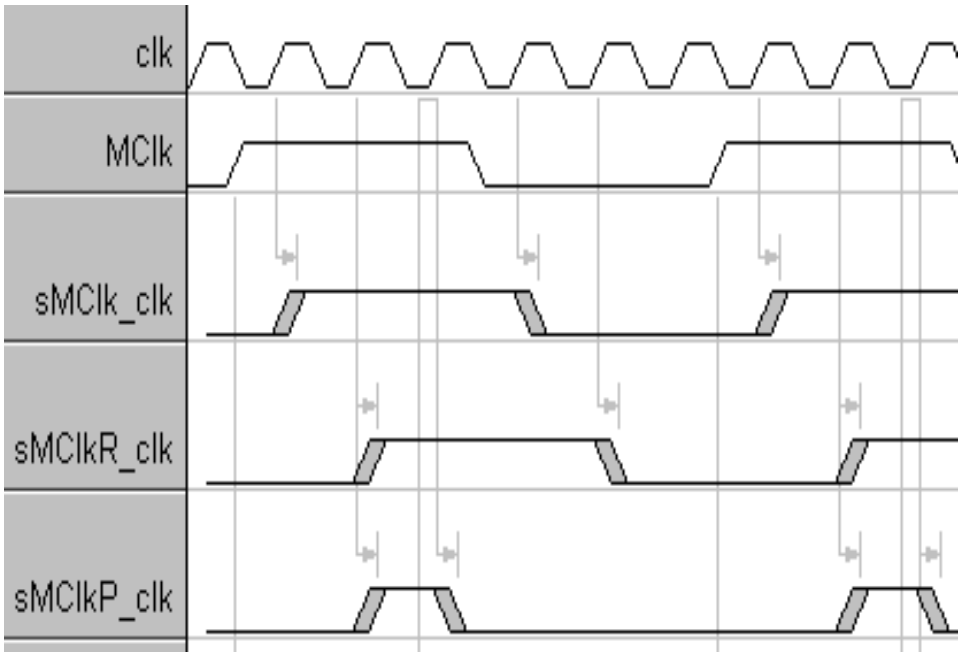
External interfaces – *camera*

- The **MCLK** (8~10MHz) has to be generated from the FPGA Clk (50 MHz in our use)
- A Clk enable internal signal is generated for use with the Clk as validating signal for the camera provided signals synchronization:
  - HSync, Data from camera
  - VSync (direction depend on the video/snapshot mode)

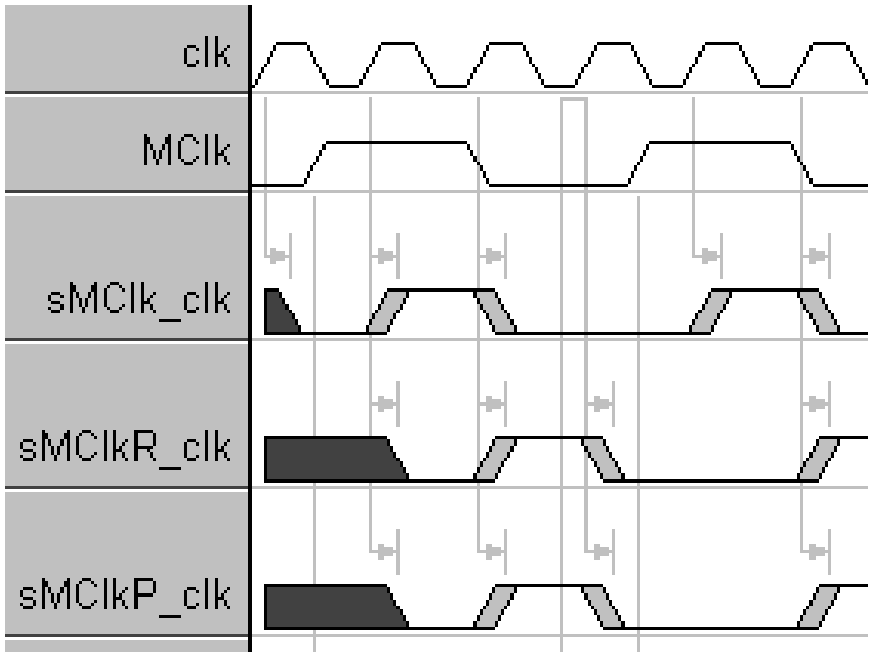
External interfaces – *camera*

- The **HSync**, **VSync**, **Data[7..0]** from camera are available between 10~25 ns after **MCLK** ↑
- As the **Clk** has a period of 20 ns → care needs to be taken for data catching/synchronization to avoid metastability problems
- A pulse of 1 clk width generated later than 40 ns after **Clk** ↑ has to be generated and used as:
  - `If rising_edge(clk) then`
  - `  if sMCLK = '1' then`
  - `  .. .. ..`
- ~ equivalent, but fully synchronous, as:
  - `if rising_edge(sMCLK) then  -- bad !!!`

Clk extraction-synchronisation



Clk/6

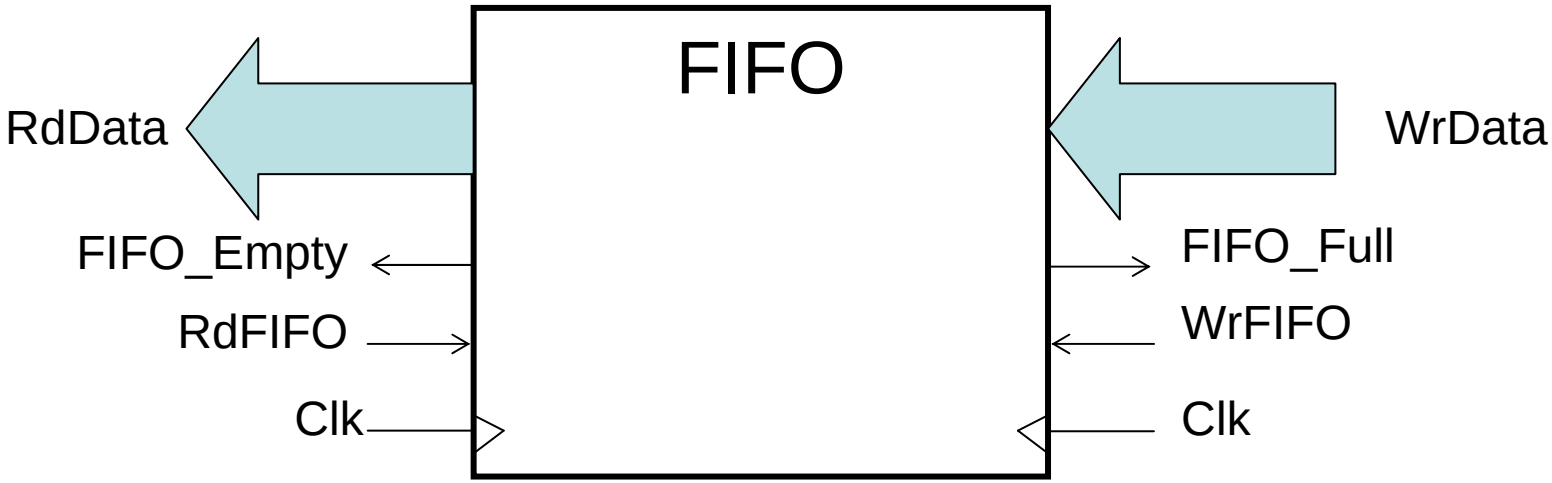


Clk/3

- MClk is generated from Clk and send to the camera sensor
- sMClk_clk and sMClkR_clk are MClk resynchronized with DFF by clk
- sMClkP_clk is a generated clock enable to be used with clk

Interface Camera, FIFO

- A FIFO (First In First Out) Memory allows the synchronization between a data producer and a data reader with asynchronous transfers rate.
- Available and configurable with QuartusII MegaWizard



Work to do…

- Analysis and realization of the camera interface
  - Avalon Slave, registers interface R/W
  - Avalon Master, master of transfers in memory
  - Camera data transfers :
    - Clock generation/synchronization from external data/signals
    - Data assembly 4 * 8 → 32 bits
    - Data in FIFO
    - Data synchronization → Avalon master
- VHDL
- Module simulation
- System on FPGA realization
- Integration in FPGA system (SDRAM, …)

Other camera interfaces

- Camera chips are available with:
  - PAL/NTSC analogue output
  - LVDS high speed serial/parallel interface
  - USB integrated interface