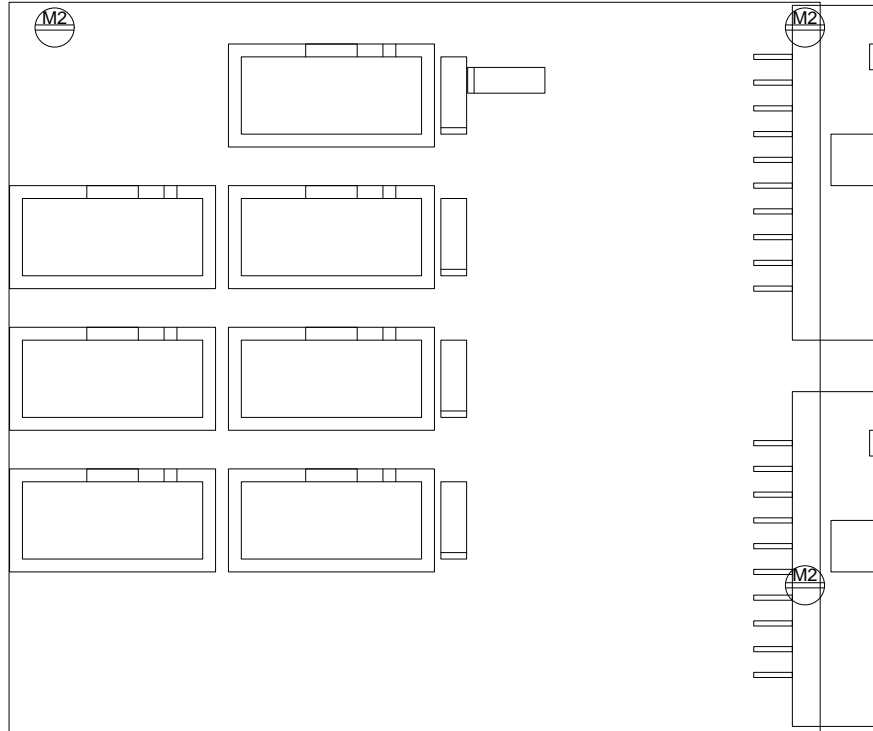


# FPGA4UEXTPAR\_B

LAP R.Beuchat  
Phone: +41 21 693 3903  
Mon Oct 29 09:55:14 MET 2007

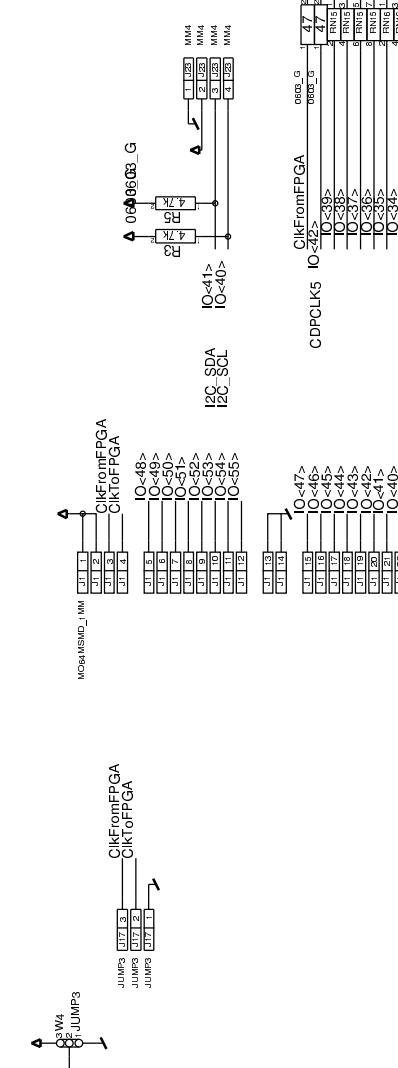
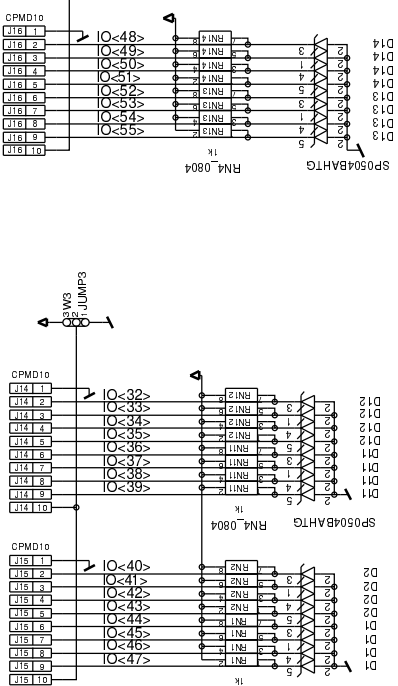
MFG\_DATE: 29.10.2007  
QUANTITY: 5  
SOLDERMASK: mtop mbot  
MATERIAL: FR4 : 1.6 mm



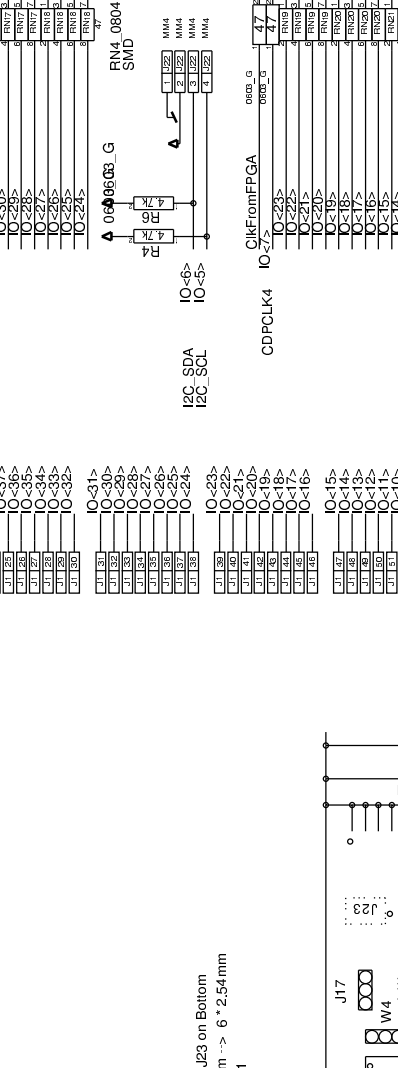
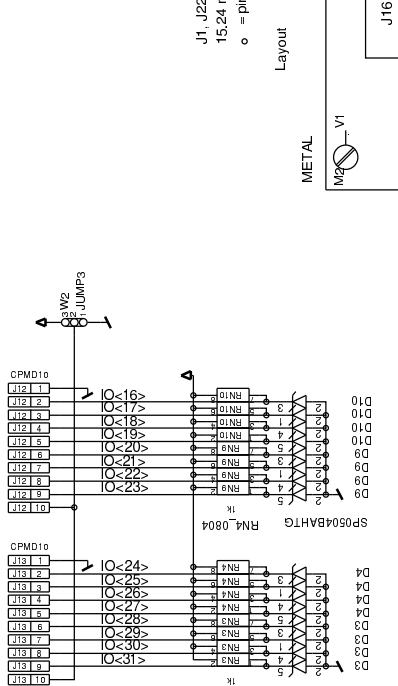
CONTENTS	PAGE
Root Schema fpga4uextpar	2 - 3
Xref fpga4uextpar	4
Drill	5
Etch	6
FPGA4U	7
OutDetail_Bottom	8
OutDetail_Top	9
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Gerber_mtop	11
Gerber_top	12
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NC-Pins Report	19
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A mettre sur le TOP

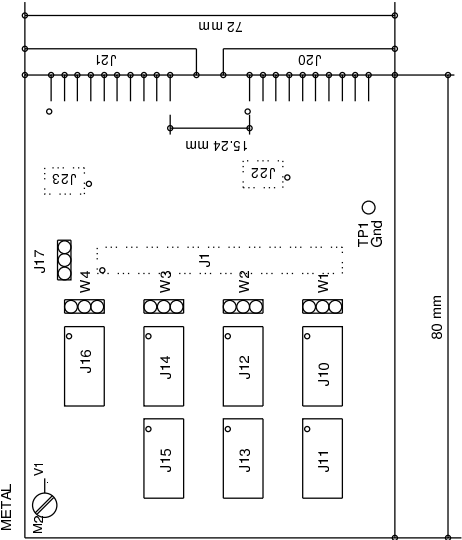


A mettre sur le TOP



J1, J22, J23 on Bottom  
15,24 mm --> 6 \* 2,54mm  
o = pin 1

Layout



A mettre sur le BOTTOM



FPGA4U Extension connector  
Adaptors for 7 x 10 pins connectors  
Adaptors for 2 x 20 pins connectors

DRAWING	ENGINEER:
FPGA4UEXTPAR_B	R. Beuchat
DATE:	PAGE:
Mon Oct 29 08:01:17 2007	1/1
	acort cuser

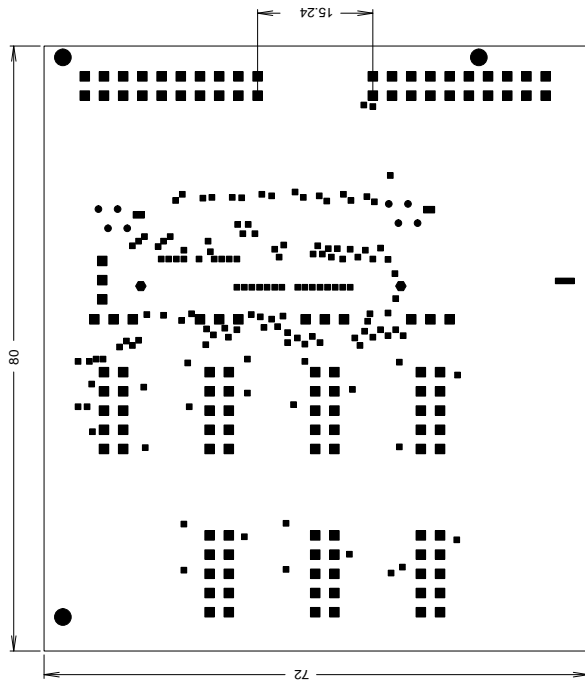
# Signal Page Ref FPGA4UEXTPAR\_B

fpga4uextpar

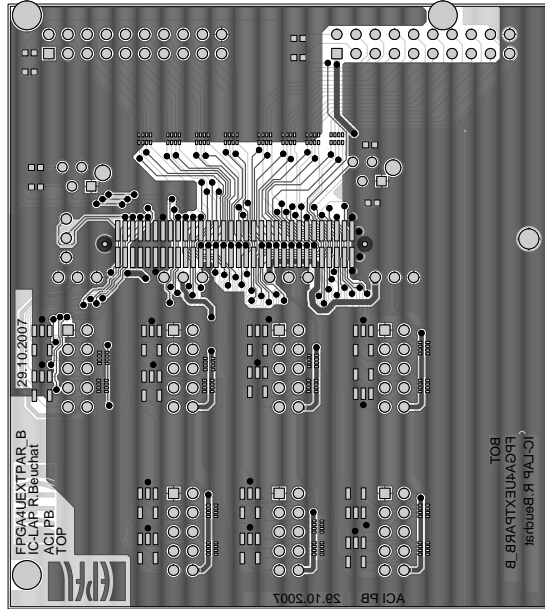
Mon Oct 29 09:55:19 MET 2007

Ref Des	Pages					
ClkFromFPGA	1	1	1	1	1%	1%
ClkToFPGA	1	1	1%	1%		
IO<0>	1	1	1%	1%		
IO<1>	1	1	1%	1%		
IO<2>	1	1	1%	1%		
IO<3>	1	1	1%	1%		
IO<4>	1	1	1%	1%		
IO<5>	1	1	1	1%	1%	
IO<6>	1	1	1	1%	1%	
IO<7>	1	1	1	1%	1%	
IO<8>	1	1	1	1%	1%	
IO<9>	1	1	1	1%	1%	
IO<10>	1	1	1	1%	1%	
IO<11>	1	1	1	1%	1%	
IO<12>	1	1	1	1%	1%	
IO<13>	1	1	1	1%	1%	
IO<14>	1	1	1	1%	1%	
IO<15>	1	1	1	1%	1%	
IO<16>	1	1	1	1%	1%	
IO<17>	1	1	1	1%	1%	
IO<18>	1	1	1	1%	1%	
IO<19>	1	1	1	1%	1%	
IO<20>	1	1	1	1%	1%	
IO<21>	1	1	1	1%	1%	
IO<22>	1	1	1	1%	1%	
IO<23>	1	1	1	1%	1%	
IO<24>	1	1	1	1%	1%	
IO<25>	1	1	1	1%	1%	
IO<26>	1	1	1	1%	1%	
IO<27>	1	1	1	1%	1%	
IO<28>	1	1	1	1%	1%	
IO<29>	1	1	1	1%	1%	
IO<30>	1	1	1	1%	1%	
IO<31>	1	1	1	1%	1%	
IO<32>	1	1	1	1%	1%	
IO<33>	1	1	1	1%	1%	
IO<34>	1	1	1	1%	1%	
IO<35>	1	1	1	1%	1%	
IO<36>	1	1	1	1%	1%	
IO<37>	1	1	1	1%	1%	
IO<38>	1	1	1	1%	1%	
IO<39>	1	1	1	1%	1%	
IO<40>	1	1	1	1%	1%	
IO<41>	1	1	1	1%	1%	
IO<42>	1	1	1	1%	1%	
IO<43>	1	1	1%	1%		
IO<44>	1	1	1%	1%		
IO<45>	1	1	1%	1%		
IO<46>	1	1	1%	1%		
IO<47>	1	1	1%	1%		
IO<48>	1	1	1%	1%		
IO<49>	1	1	1%	1%		
IO<50>	1	1	1%	1%		
IO<51>	1	1	1%	1%		
IO<52>	1	1	1%	1%		
IO<53>	1	1	1%	1%		
IO<54>	1	1	1%	1%		
IO<55>	1	1	1%	1%		

Total Signals count 58



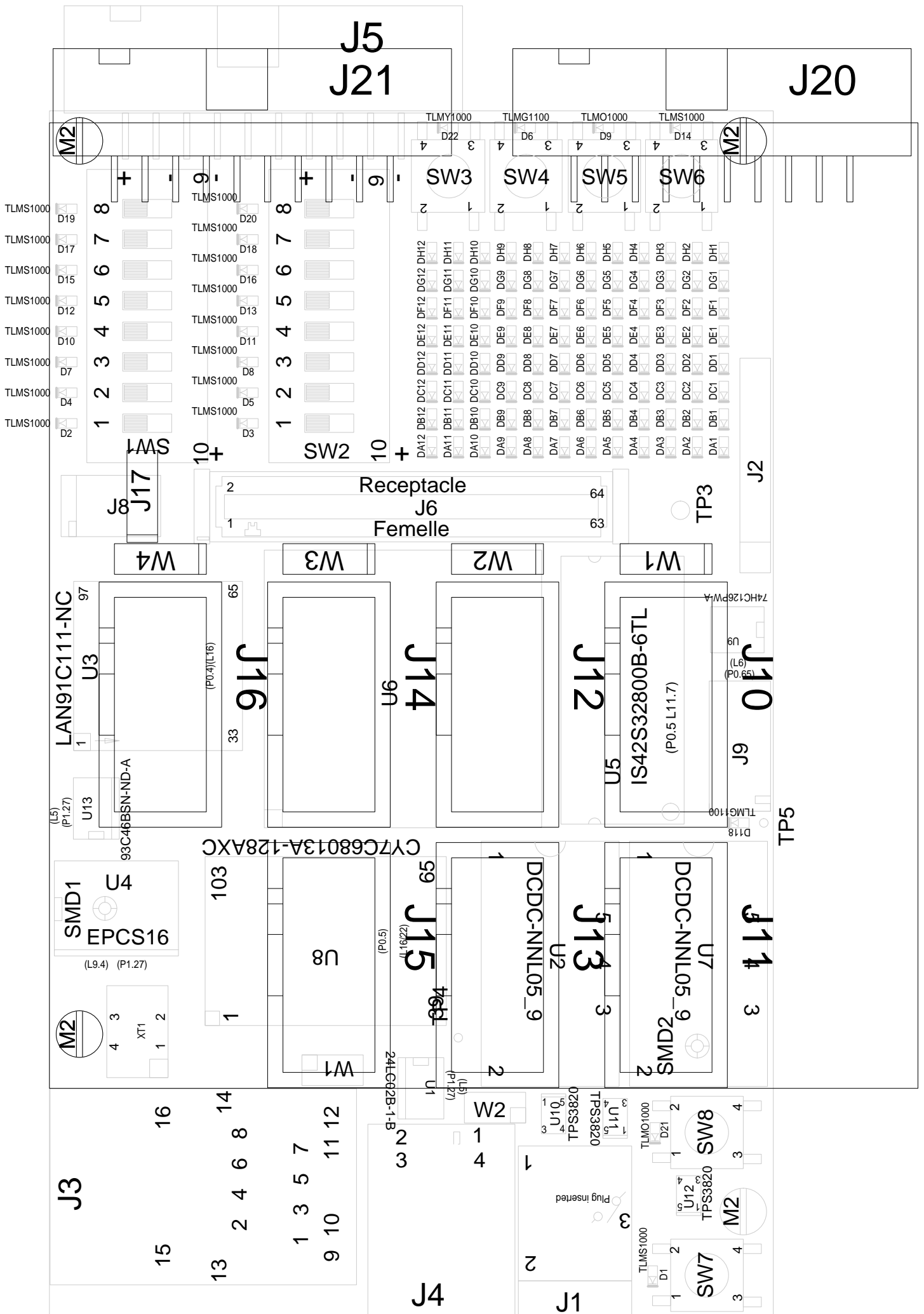
DRILL CHART		
FIGURE	SIZE	QTY
•	0.301	140
◦	0.787	8
◻	0.889	125
◻	0.94	1
◻	1.499	2
●	2.2	3
●	1.4	NOT PLATED

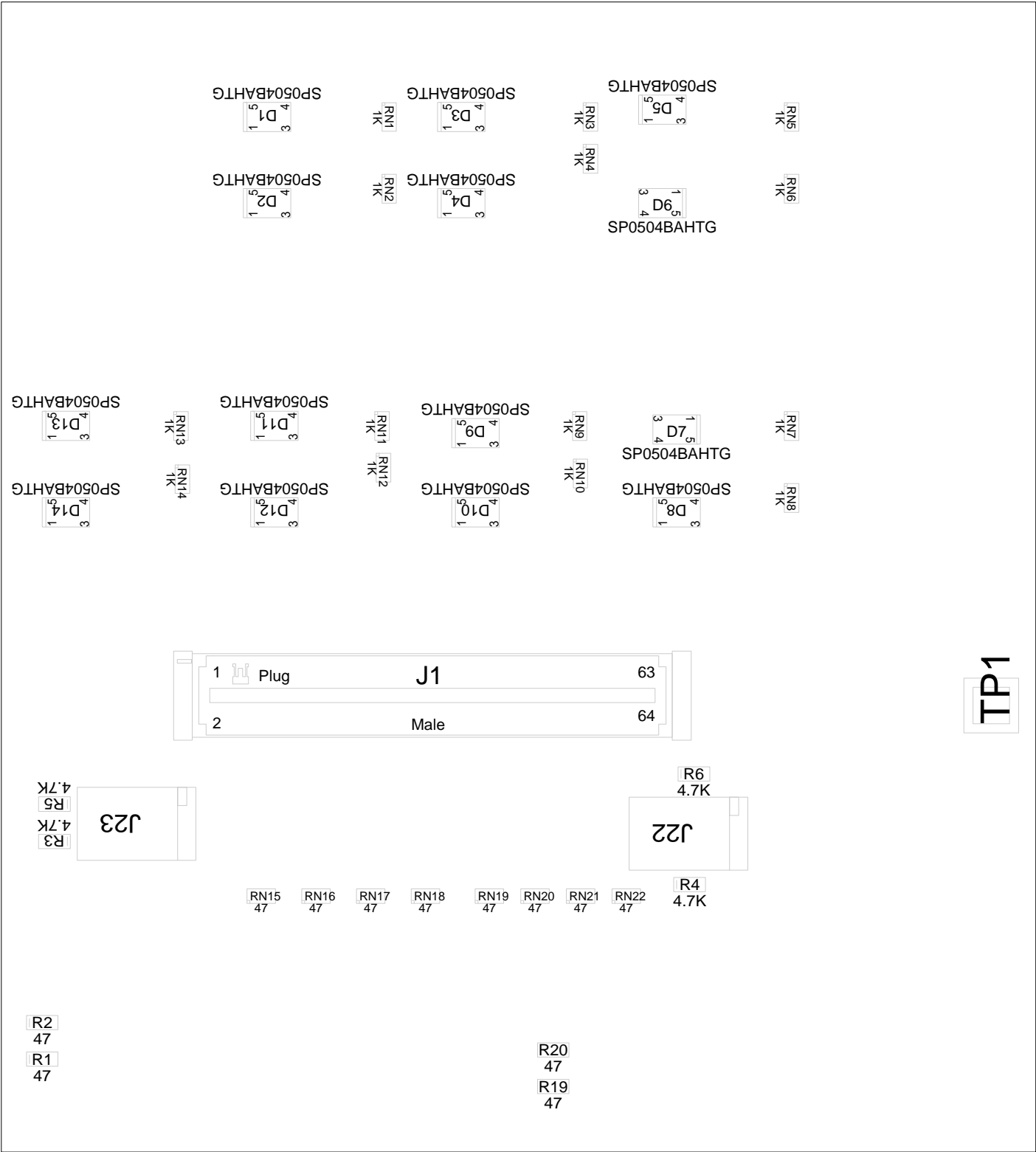


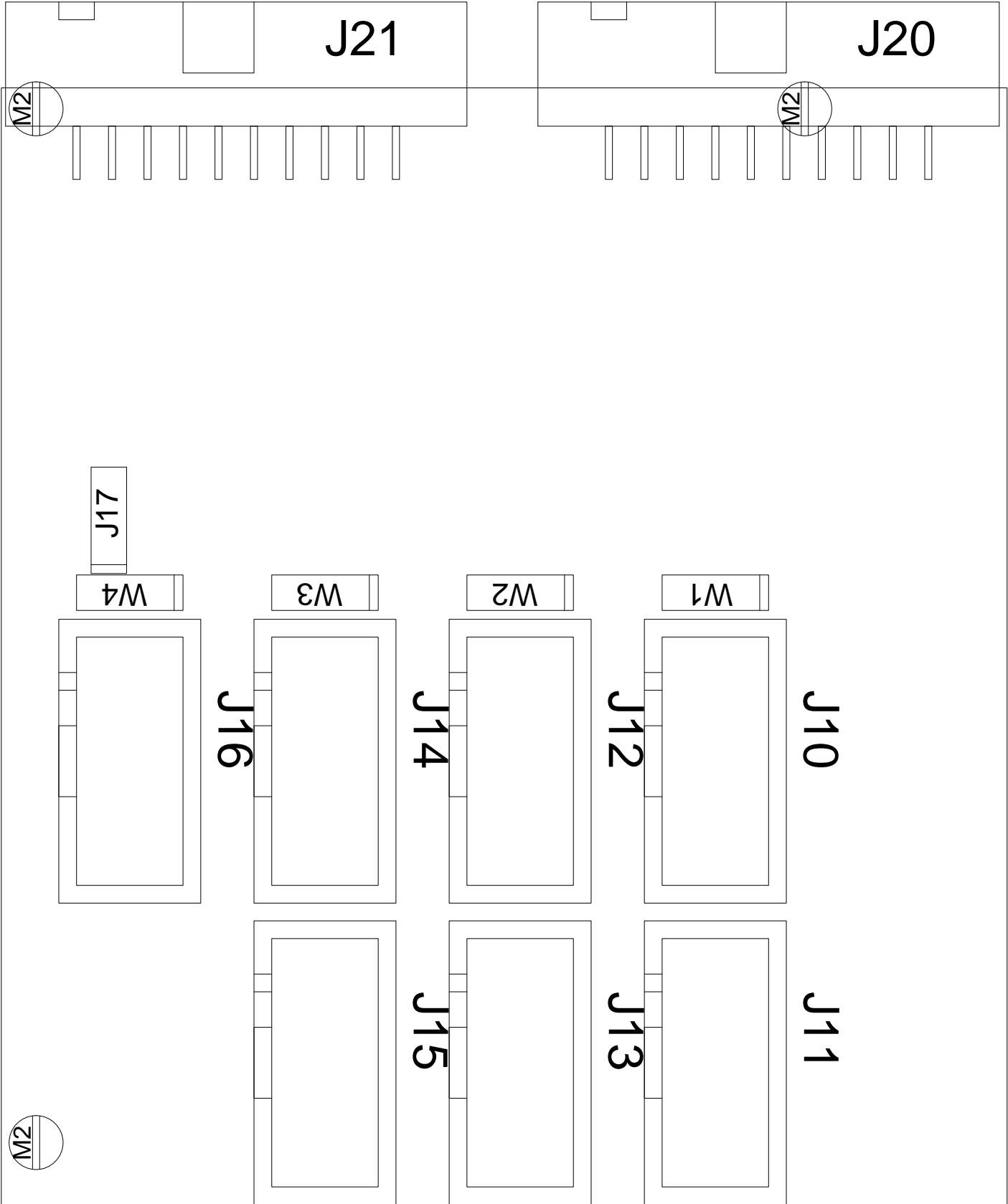
TITRE:FPGA4UXTPAR

LABORATOIRE:IC-LAP  
ENGINEER:R.Beuchat

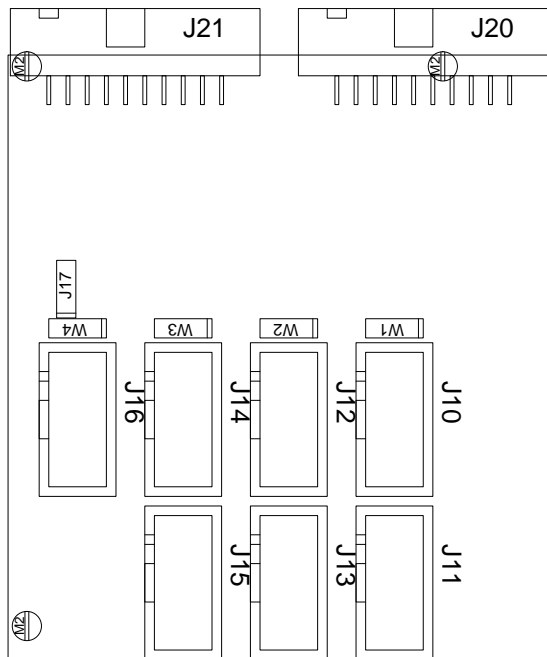
DATE:24.8.2007  
EPFL-ACORT-PB

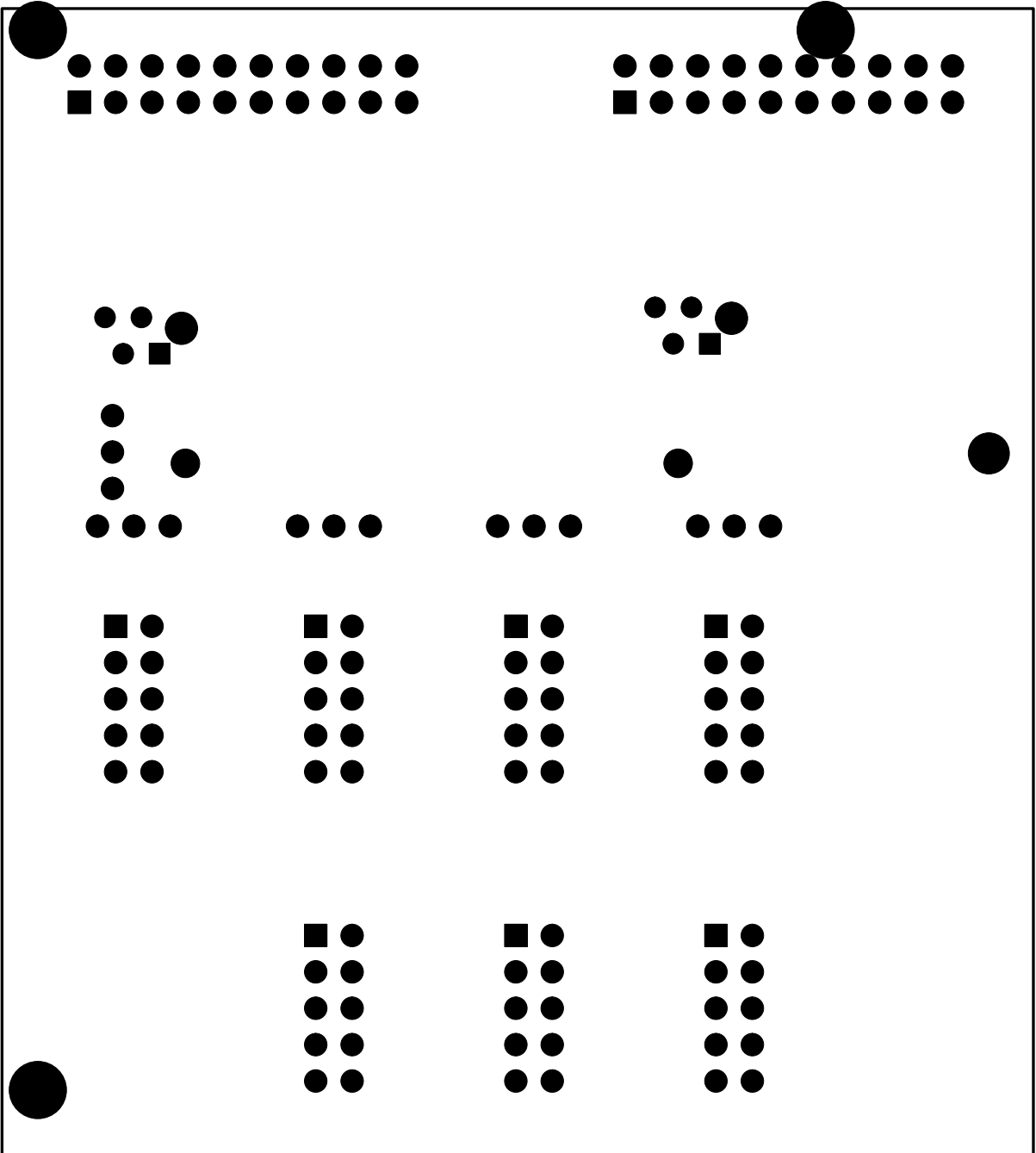


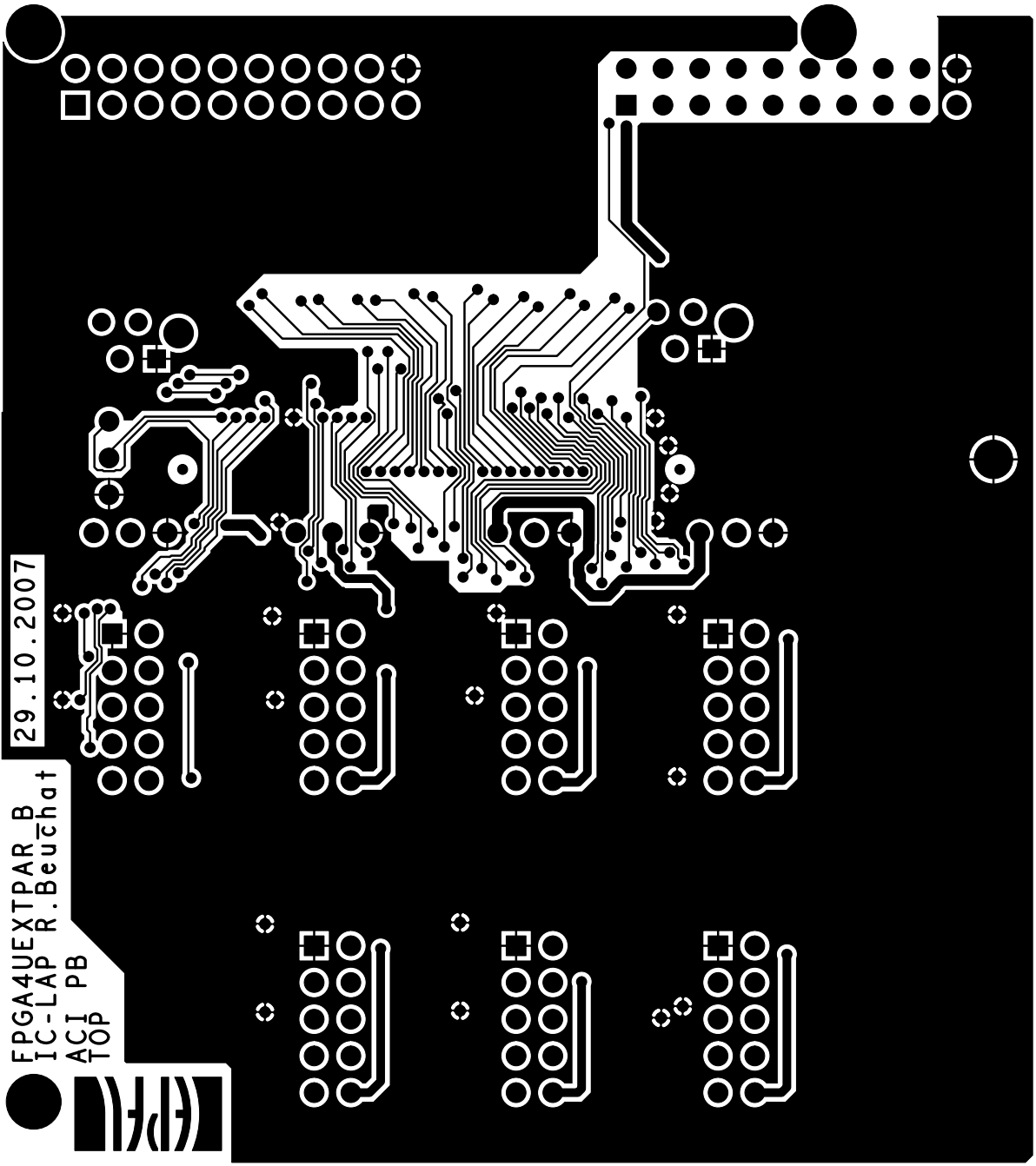






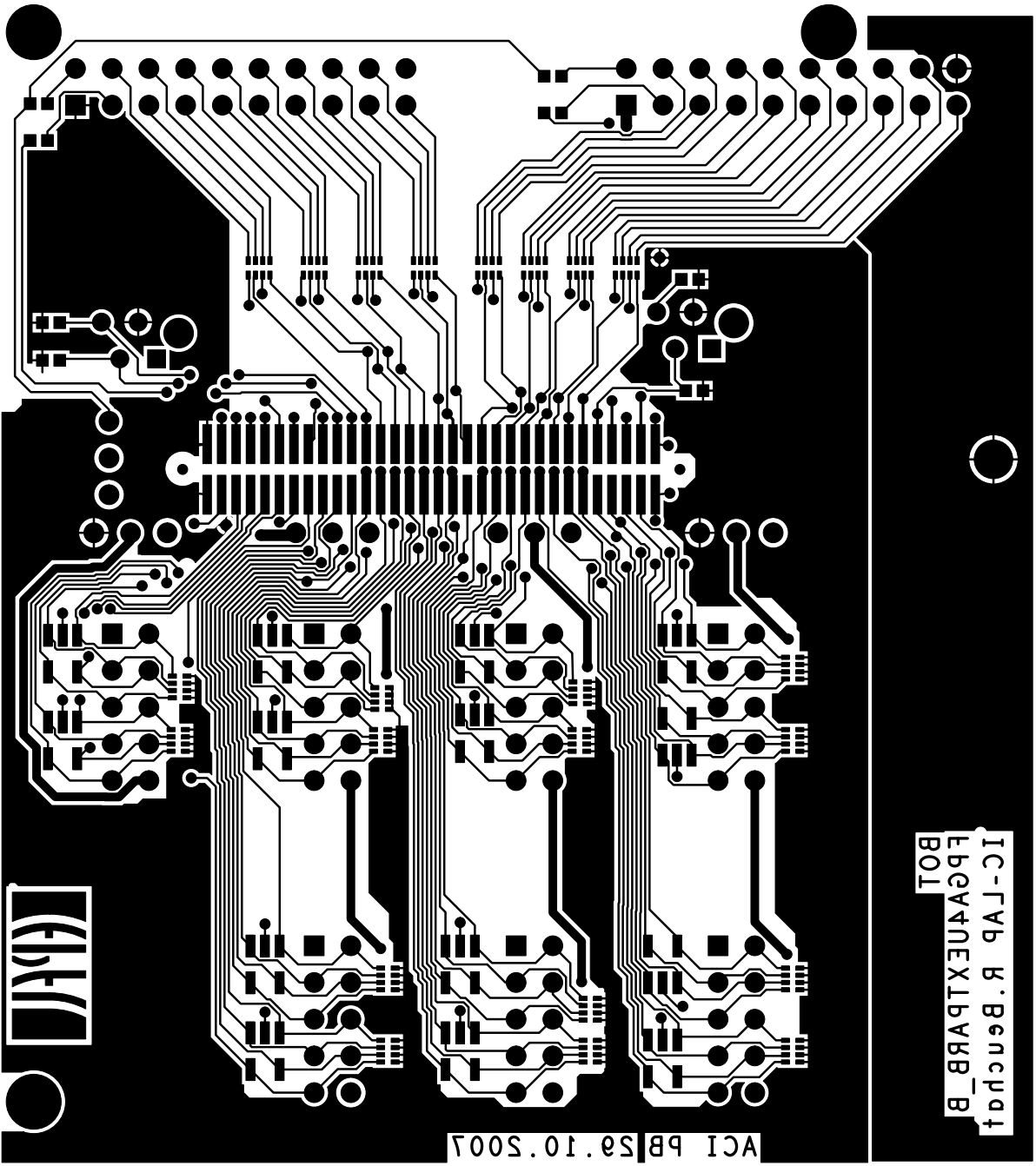






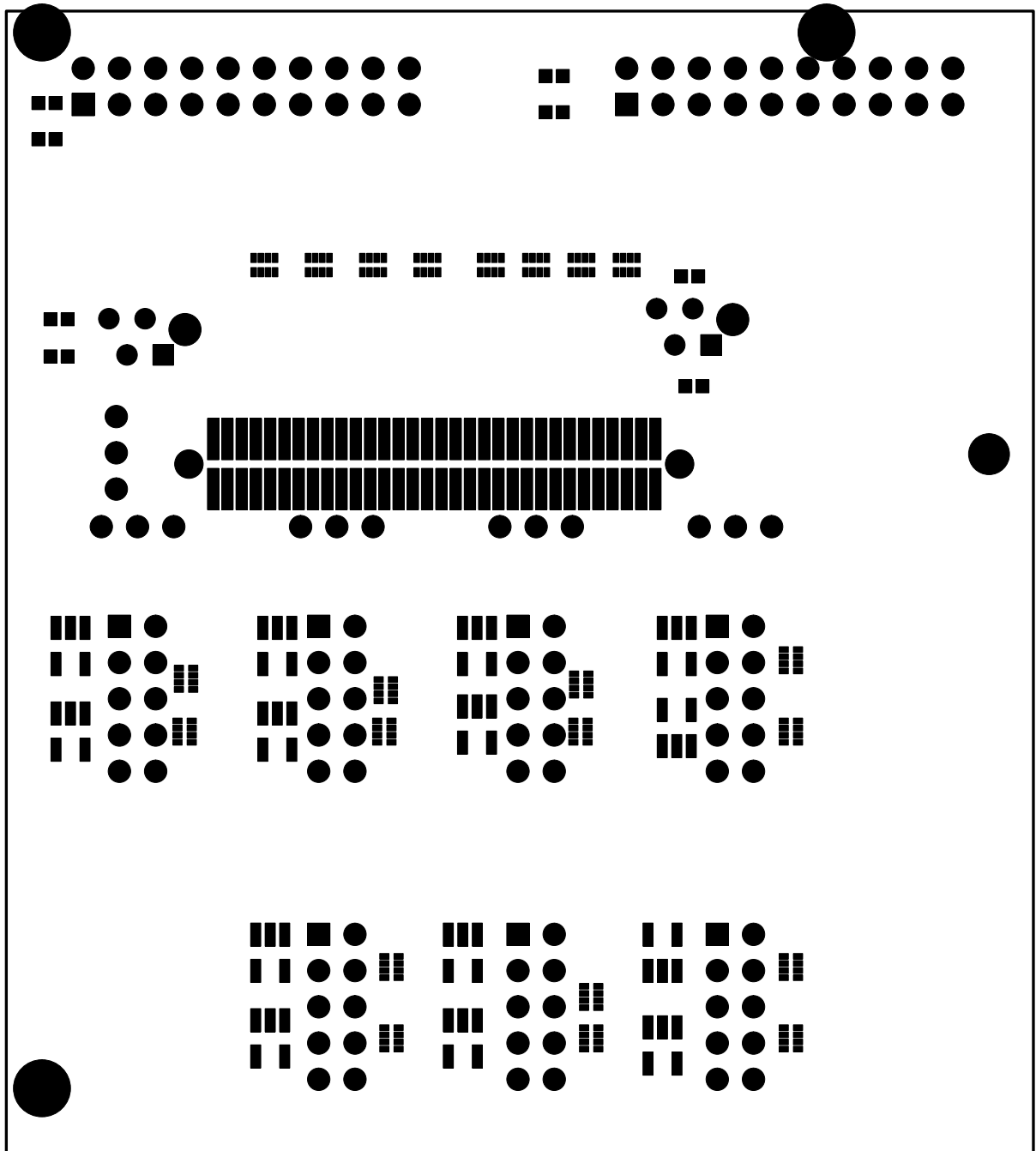
29.10.2007

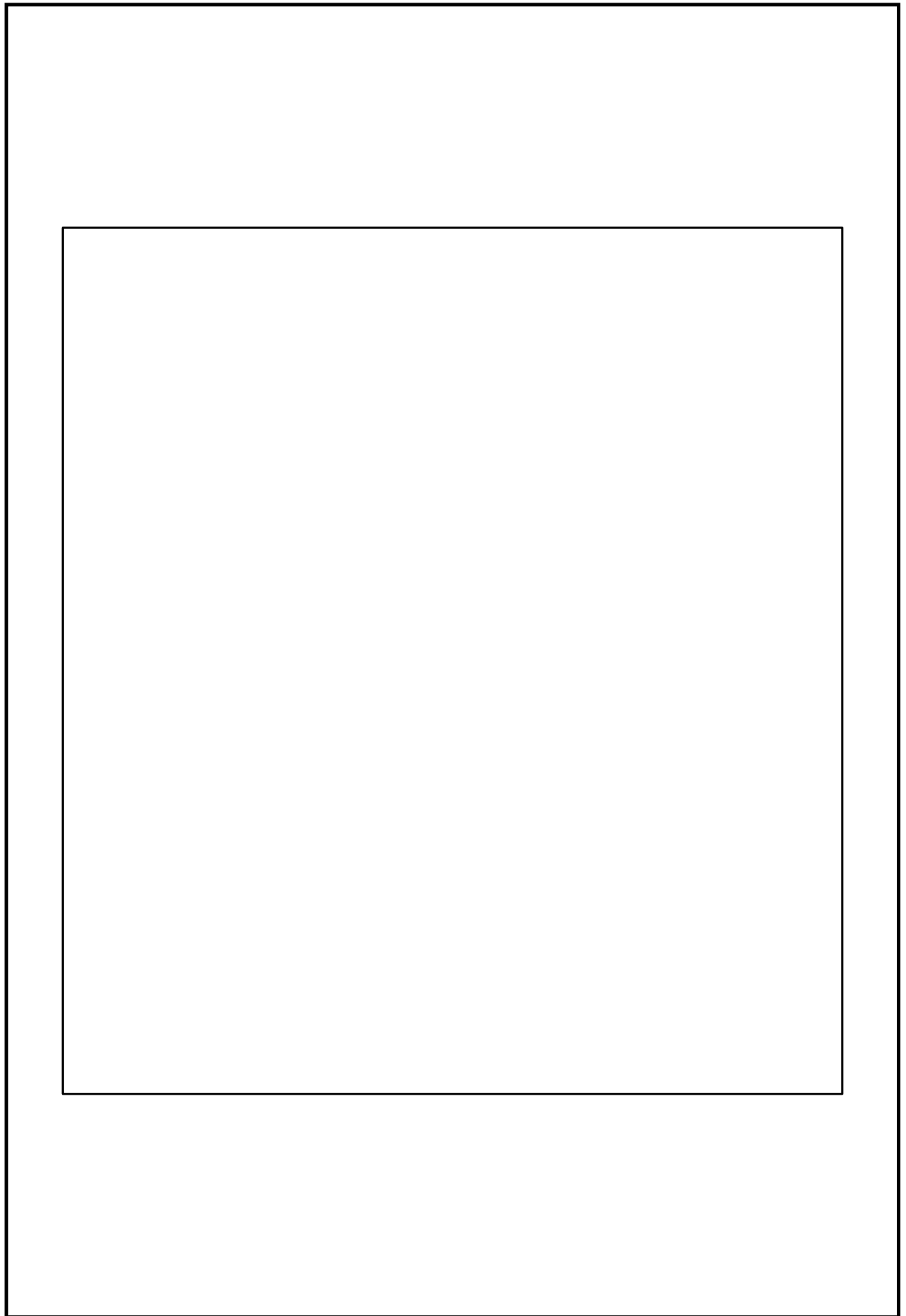
FPGA4UEXTPAR\_B  
IC-LAP R. Beuchat  
ACI PB  
TOP



ACI PB | Sa. 10.5007

IC-Tab. R. Benchpa  
FbGV4NEX1PVRB\_B  
B01





# Component Report FPGA4UEXTPAR\_B

fpga4uextparb\_gloss

Mon Oct 29 09:55:19 MET 2007

Ref Des	Device Type	Value	Package Type	x	y	ang	Mir	Remark
D1	SP0504BAHTG	SP0504BAHTG	SOT23_5	27.000	41.500	0.000	YES	
D2	SP0504BAHTG	SP0504BAHTG	SOT23_5	33.000	41.500	0.000	YES	
D3	SP0504BAHTG	SP0504BAHTG	SOT23_5	27.000	28.000	0.000	YES	
D4	SP0504BAHTG	SP0504BAHTG	SOT23_5	33.000	28.000	0.000	YES	
D5	SP0504BAHTG	SP0504BAHTG	SOT23_5	26.500	14.000	0.000	YES	
D6	SP0504BAHTG	SP0504BAHTG	SOT23_5	33.000	14.000	180.000	YES	
D7	SP0504BAHTG	SP0504BAHTG	SOT23_5	48.750	13.000	180.000	YES	
D8	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	13.000	0.000	YES	
D9	SP0504BAHTG	SP0504BAHTG	SOT23_5	49.000	27.000	0.000	YES	
D10	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	27.000	0.000	YES	
D11	SP0504BAHTG	SP0504BAHTG	SOT23_5	48.500	41.000	0.000	YES	
D12	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	41.000	0.000	YES	
D13	SP0504BAHTG	SP0504BAHTG	SOT23_5	48.500	55.500	0.000	YES	
D14	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	55.500	0.000	YES	
J1	CO64		MO64MSMD_1MM	67.250	30.000	90.000	YES	
J10	CO10		CPMD10	55.880	10.160	180.000	NO	
J11	CO10		CPMD10	34.290	10.160	180.000	NO	
J12	CO10		CPMD10	55.880	24.130	180.000	NO	
J13	CO10		CPMD10	34.290	24.130	180.000	NO	
J14	CO10		CPMD10	55.880	38.100	180.000	NO	
J15	CO10		CPMD10	34.290	38.100	180.000	NO	
J16	CO10		CPMD10	55.880	52.070	180.000	NO	
J17	CO3		JUMP3	65.500	49.750	0.000	NO	
J20	CO20		CPMC20	92.450	16.510	270.000	NO	
J21	CO20		CPMC20	92.450	54.610	270.000	NO	
J22	CO4		MM4	75.600	10.600	270.000	YES	
J23	CO4		MM4	74.900	49.000	270.000	YES	
R1	R	47	0603_G	92.550	57.150	0.000	YES	
R2	R	47	0603_G	90.010	57.150	0.000	YES	
R3	R	4.7K	0603_G	77.400	56.300	180.000	YES	
R4	R	4.7K	0603_G	80.400	12.100	0.000	YES	
R5	R	4.7K	0603_G	74.800	56.300	180.000	YES	
R6	R	4.7K	0603_G	72.700	11.800	0.000	YES	
R19	R	47	0603_G	94.455	21.590	0.000	YES	
R20	R	47	0603_G	91.915	21.590	0.000	YES	
RN1	RN0805	1K	RN4_0804	27.000	33.000	90.000	YES	
RN2	RN0805	1K	RN4_0804	32.000	33.000	90.000	YES	
RN3	RN0805	1K	RN4_0804	27.000	19.000	90.000	YES	
RN4	RN0805	1K	RN4_0804	29.900	19.000	90.000	YES	
RN5	RN0805	1K	RN4_0804	27.000	5.000	90.000	YES	
RN6	RN0805	1K	RN4_0804	32.000	5.000	90.000	YES	
RN7	RN0805	1K	RN4_0804	48.500	5.000	90.000	YES	
RN8	RN0805	1K	RN4_0804	53.500	5.000	90.000	YES	
RN9	RN0805	1K	RN4_0804	48.500	19.750	90.000	YES	
RN10	RN0805	1K	RN4_0804	51.800	19.700	90.000	YES	
RN11	RN0805	1K	RN4_0804	48.500	33.500	90.000	YES	
RN12	RN0805	1K	RN4_0804	51.400	33.400	90.000	YES	
RN13	RN0805	1K	RN4_0804	48.500	47.500	90.000	YES	
RN14	RN0805	1K	RN4_0804	52.200	47.400	90.000	YES	
RN15	RN0805	47	RN4_0804	81.200	41.910	0.000	YES	
RN16	RN0805	47	RN4_0804	81.200	38.100	0.000	YES	
RN17	RN0805	47	RN4_0804	81.200	34.290	0.000	YES	
RN18	RN0805	47	RN4_0804	81.200	30.480	0.000	YES	
RN19	RN0805	47	RN4_0804	81.200	26.035	0.000	YES	
RN20	RN0805	47	RN4_0804	81.200	22.860	0.000	YES	
RN21	RN0805	47	RN4_0804	81.200	19.685	0.000	YES	
RN22	RN0805	47	RN4_0804	81.200	16.510	0.000	YES	
TP1	TP		TPLOGI	67.945	-8.890	0.000	YES	

# Component Report FPGA4UEXTPAR\_B

fpga4uextparb\_gloss

Mon Oct 29 09:55:19 MET 2007

Ref Des	Device Type	Value	Package Type	x	y	ang	Mir	Remark
V1	VIS_METAL		VIS2	23.500	57.500	0.000	NO	
W1	JUMP3		JUMP3	65.405	6.350	90.000	NO	
W2	JUMP3		JUMP3	65.405	20.320	90.000	NO	
W3	JUMP3		JUMP3	65.405	34.290	90.000	NO	
W4	JUMP3		JUMP3	65.405	48.260	90.000	NO	

Total Component count 63



# BOM Report FPGA4UEXTPAR\_B

fpga4uextparb\_gloss

Mon Oct 29 09:55:20 MET 2007

Device	Package	Value	Nb	Reference Designators					Remark
CO10-CPMD10	CPMD10		7	J10 J15	J11 J16	J12	J13	J14	
CO20-CPMC20	CPMC20		2	J20	J21				
CO3-JUMP3	JUMP3		1	J17					
CO4-MM4	MM4		2	J22	J23				
CO64-MO64MSMD_1MM	MO64MSMD_1MM		1	J1					
JUMP3-1	JUMP3		4	W1	W2	W3	W4		
R-0603_G-4.7K	0603_G	4.7K	4	R3	R4	R5	R6		
R-0603_G-47	0603_G	47	4	R1	R2	R19	R20		
RN0805-1-1K	RN4_0804	1K	14	RN1 RN6 RN11	RN2 RN7	RN3 RN8 RN13	RN4 RN9 RN14	RN5 RN10	
RN0805-1-47	RN4_0804	47	8	RN15 RN20	RN16 RN21	RN17 RN22	RN18	RN19	
SP0504BAHTG-SP0504BA	SOT23_5	SP0504BAHTG	4	D1 D6 D11	D2 D7	D3 D8 D13	D4 D9 D14	D5 D10	
TP-4	TPLOGI		1	TP1					
VIS_METAL-M2	VIS2		1	V1					

Total Component count 63

# NC Pins Report FPGA4UEXTPAR\_B

fpga4uextparb\_gloss

Mon Oct 29 09:55:20 MET 2007

Ref Des	Device	Nb	Not Connected Pins	Remark
V1	VIS_METAL-M2	1	1	

Total count 1

# Power Pins Report FPGA4UEXTPAR\_B

fpga4uextparb\_gloss

Mon Oct 29 09:55:21 MET 2007

Ref Des	Device	Name	Power Pins	Remark
D1	SP0504BAHTG-SP0504BA	GND	2	
D2	SP0504BAHTG-SP0504BA	GND	2	
D3	SP0504BAHTG-SP0504BA	GND	2	
D4	SP0504BAHTG-SP0504BA	GND	2	
D5	SP0504BAHTG-SP0504BA	GND	2	
D6	SP0504BAHTG-SP0504BA	GND	2	
D7	SP0504BAHTG-SP0504BA	GND	2	
D8	SP0504BAHTG-SP0504BA	GND	2	
D9	SP0504BAHTG-SP0504BA	GND	2	
D10	SP0504BAHTG-SP0504BA	GND	2	
D11	SP0504BAHTG-SP0504BA	GND	2	
D12	SP0504BAHTG-SP0504BA	GND	2	
D13	SP0504BAHTG-SP0504BA	GND	2	
D14	SP0504BAHTG-SP0504BA	GND	2	
J1	CO64-MO64MSMD_1MM	GND	13 14 63 64	
		VCC	1 2	
J10	CO10-CPMD10	GND	1	
J11	CO10-CPMD10	GND	1	
J12	CO10-CPMD10	GND	1	
J13	CO10-CPMD10	GND	1	
J14	CO10-CPMD10	GND	1	
J15	CO10-CPMD10	GND	1	
J16	CO10-CPMD10	GND	1	
J17	CO3-JUMP3	GND	1 20	
J20	CO20-CPMC20	VCC	1	
J21	CO20-CPMC20	GND	20	
		VCC	1	
J22	CO4-MM4	GND	1	
		VCC	2	
J23	CO4-MM4	GND	1	
		VCC	2	
RN1	RN0805-1-1K	VCC	2 4 6 8	
RN2	RN0805-1-1K	VCC	2 4 6 8	
RN3	RN0805-1-1K	VCC	2 4 6 8	
RN4	RN0805-1-1K	VCC	2 4 6 8	
RN5	RN0805-1-1K	VCC	2 4 6 8	
RN6	RN0805-1-1K	VCC	2 4 6 8	
RN7	RN0805-1-1K	VCC	2 4 6 8	
RN8	RN0805-1-1K	VCC	2 4 6 8	
RN9	RN0805-1-1K	VCC	2 4 6 8	
RN10	RN0805-1-1K	VCC	2 4 6 8	
RN11	RN0805-1-1K	VCC	2 4 6 8	
RN12	RN0805-1-1K	VCC	2 4 6 8	
RN13	RN0805-1-1K	VCC	2 4 6 8	
RN14	RN0805-1-1K	VCC	2 4 6 8	
TP1	TP-4	GND	1	
W1	JUMP3-1	GND	1	
		VCC	3	
W2	JUMP3-1	GND	1	
		VCC	3	
W3	JUMP3-1	GND	1	
		VCC	3	
W4	JUMP3-1	GND	1	
		VCC	3	

Total count 46

# Single Node Nets Report FPGA4UEXTPAR\_B

fpga4uextparb\_gloss

Mon Oct 29 09:55:22 MET 2007

Netname	Node	Device	Remark
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Total Nets count 0