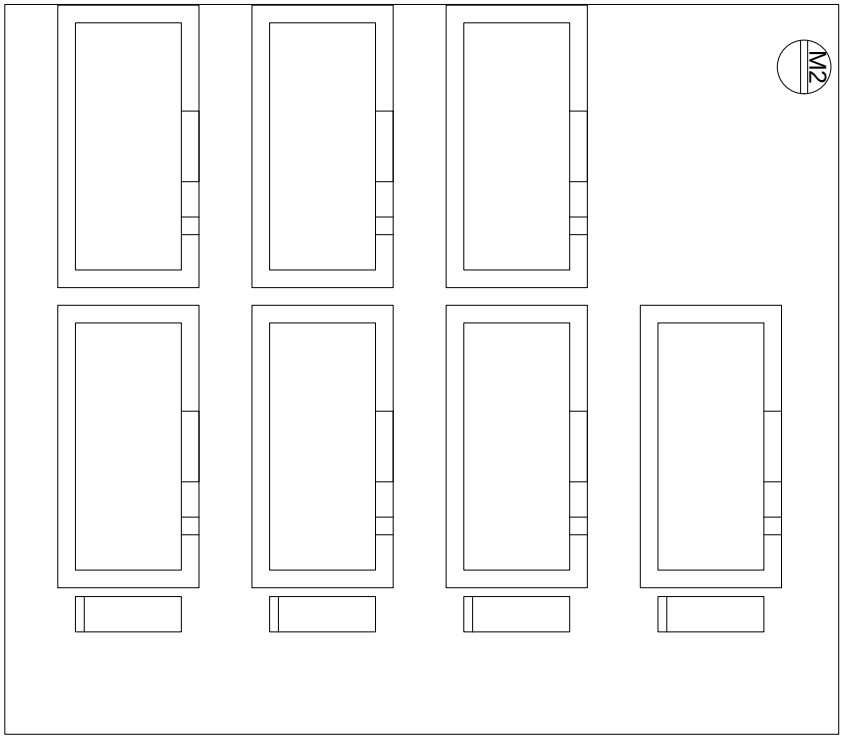
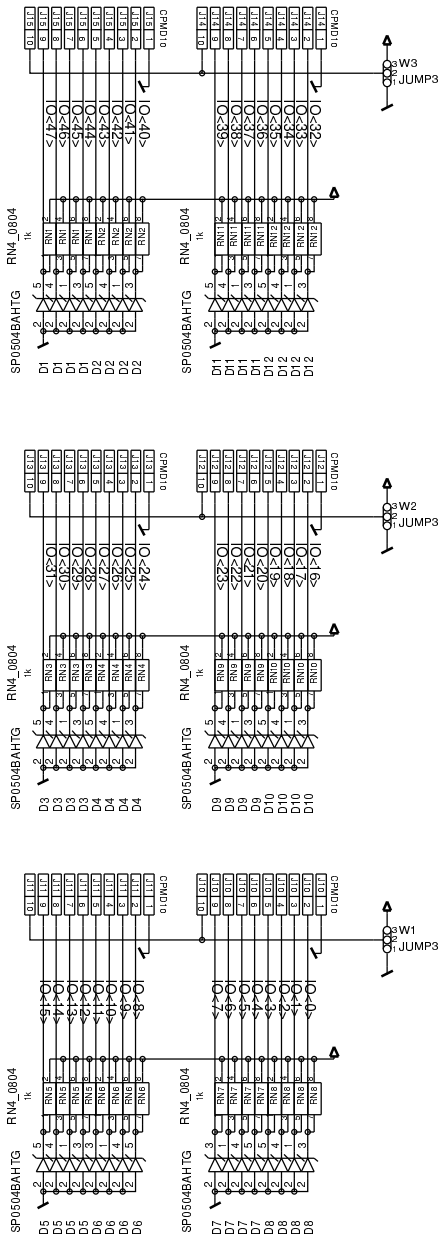
FPGA4UEXTPAR

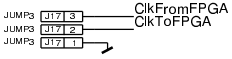
LAP R.Beuchat
Phone: +41 21 693 3903
Wed Aug 29 11:33:06 MET DST 2007

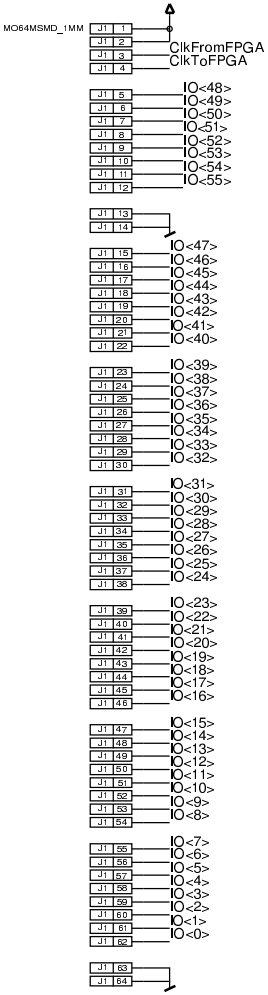
MFG_DATE: 27.08.2007
QUANTITY: 10
SOLDERMASK: mtop mbot
MATERIAL: FR4 : 1.6 mm



A mettre sur le TOP



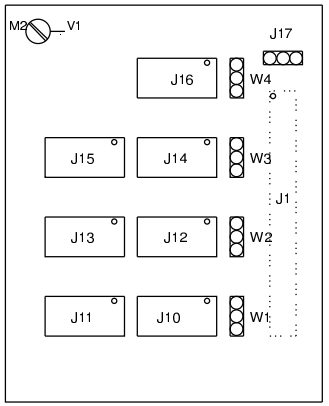




A mettre sur le BOTTOM

A mettre sur le TOP

Layout



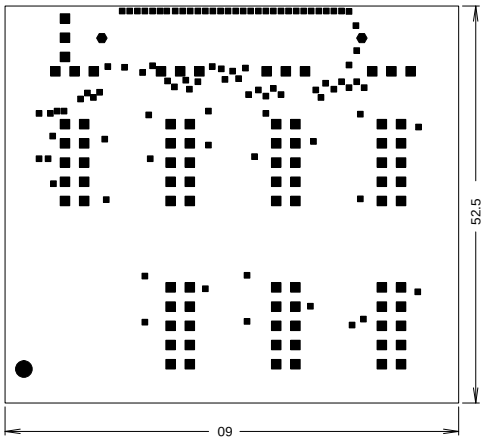
DRAWING FPGA4UEXTPAR	ENGINEER: R.Beuchat
DATE: Wed Aug 29 09:56:28 2007	PAGE: 1/1 acort cuser

Signal Page Ref FPGA4UEXTPAR

Ref Des	Pages			
ClkFromFPGA	1	1	1%	1%
ClkToFPGA	1	1	1%	1%
IO<0>	1	1	1%	1%
IO<1>	1	1	1%	1%
IO<2>	1	1	1%	1%
IO<3>	1	1	1%	1%
IO<4>	1	1	1%	1%
IO<5>	1	1	1%	1%
IO<6>	1	1	1%	1%
IO<7>	1	1	1%	1%
IO<8>	1	1	1%	1%
IO<9>	1	1	1%	1%
IO<10>	1	1	1%	1%
IO<11>	1	1	1%	1%
IO<12>	1	1	1%	1%
IO<13>	1	1	1%	1%
IO<14>	1	1	1%	1%
IO<15>	1	1	1%	1%
IO<16>	1	1	1%	1%
IO<17>	1	1	1%	1%
IO<18>	1	1	1%	1%
IO<19>	1	1	1%	1%
IO<20>	1	1	1%	1%
IO<21>	1	1	1%	1%
IO<22>	1	1	1%	1%
IO<23>	1	1	1%	1%
IO<24>	1	1	1%	1%
IO<25>	1	1	1%	1%
IO<26>	1	1	1%	1%
IO<27>	1	1	1%	1%
IO<28>	1	1	1%	1%
IO<29>	1	1	1%	1%
IO<30>	1	1	1%	1%
IO<31>	1	1	1%	1%
IO<32>	1	1	1%	1%
IO<33>	1	1	1%	1%
IO<34>	1	1	1%	1%
IO<35>	1	1	1%	1%
IO<36>	1	1	1%	1%
IO<37>	1	1	1%	1%
IO<38>	1	1	1%	1%
IO<39>	1	1	1%	1%
IO<40>	1	1	1%	1%
IO<41>	1	1	1%	1%
IO<42>	1	1	1%	1%
IO<43>	1	1	1%	1%
IO<44>	1	1	1%	1%
IO<45>	1	1	1%	1%
IO<46>	1	1	1%	1%
IO<47>	1	1	1%	1%
IO<48>	1	1	1%	1%
IO<49>	1	1	1%	1%
IO<50>	1	1	1%	1%
IO<51>	1	1	1%	1%
IO<52>	1	1	1%	1%
IO<53>	1	1	1%	1%
IO<54>	1	1	1%	1%
IO<55>	1	1	1%	1%

Total Signals count 58

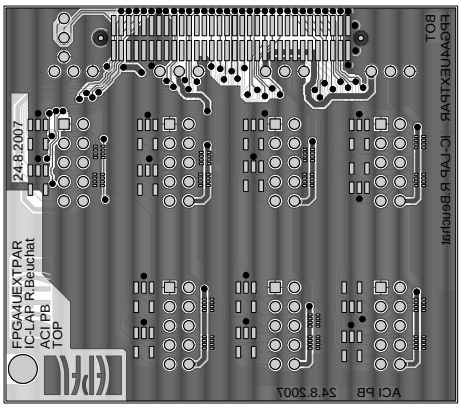
DRILL CHART			
FIGURE	SIZE	PLATED	QTY
·	0.301	PLATED	95
■	0.889	PLATED	85
●	2.2	PLATED	1
⬣	1.4	NOT PLATED	2



TITRE:FPGA4UEXTPAR

LABORATOIRE:IC-LAP	DATE:24.8.2007
ENGINEER:R.Beuchat	EPFL-ACORT-PB

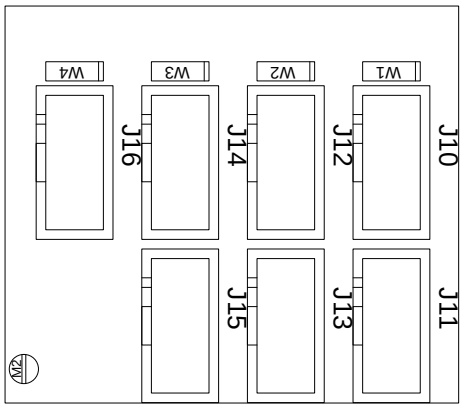
EPFL ACORT Wed 29.08.2007 11:32 Drawing name = FPGA4UEXTPAR Scale = 1.00 1.000 Inch =



TITRE:FPGA4UEXTPAR	LABORATOIRE:IC-LAP	DATE:24.8.2007
	ENGINEER:R.Beuchat	EPFL-ACORT-PB

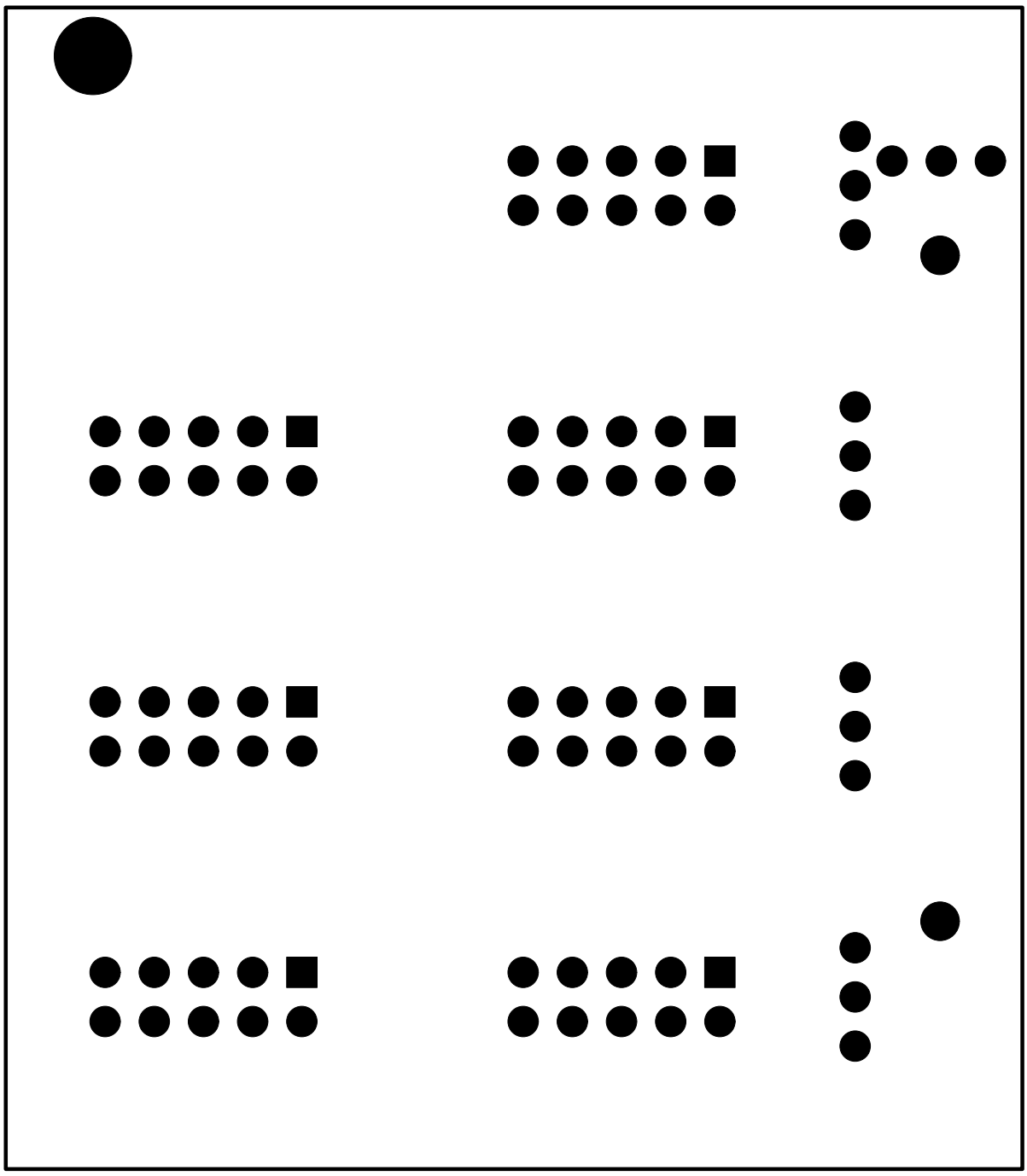
J17
J1
Male
Plug
1
2
63
64
D14
SP0504BAHTG
D13
SP0504BAHTG
RN14
1K
RN13
1K
D12
SP0504BAHTG
D11
SP0504BAHTG
D2
SP0504BAHTG
D1
SP0504BAHTG
RN12
1K
RN11
1K
RN2
1K
RN1
1K
D10
SP0504BAHTG
D9
SP0504BAHTG
D4
SP0504BAHTG
D3
SP0504BAHTG
RN10
1K
RN9
1K
RN4
1K
RN3
1K
D8
SP0504BAHTG
D7
SP0504BAHTG
D6
SP0504BAHTG
D5
SP0504BAHTG
RN8
1K
RN7
1K
RN6
1K
RN5
1K

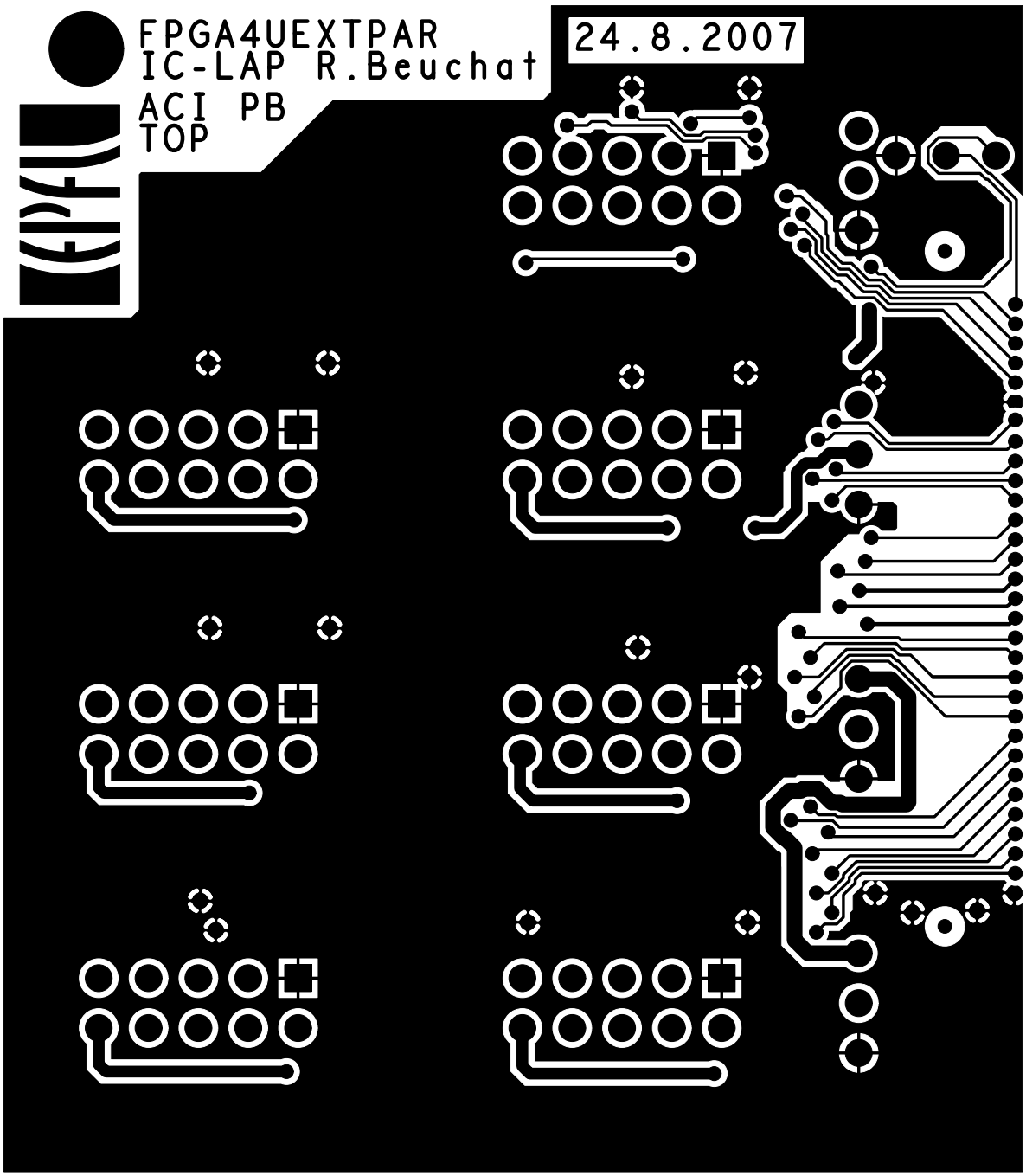
M2
W4
J16
W3
J15
J14
W2
J13
J12
W1
J11
J10

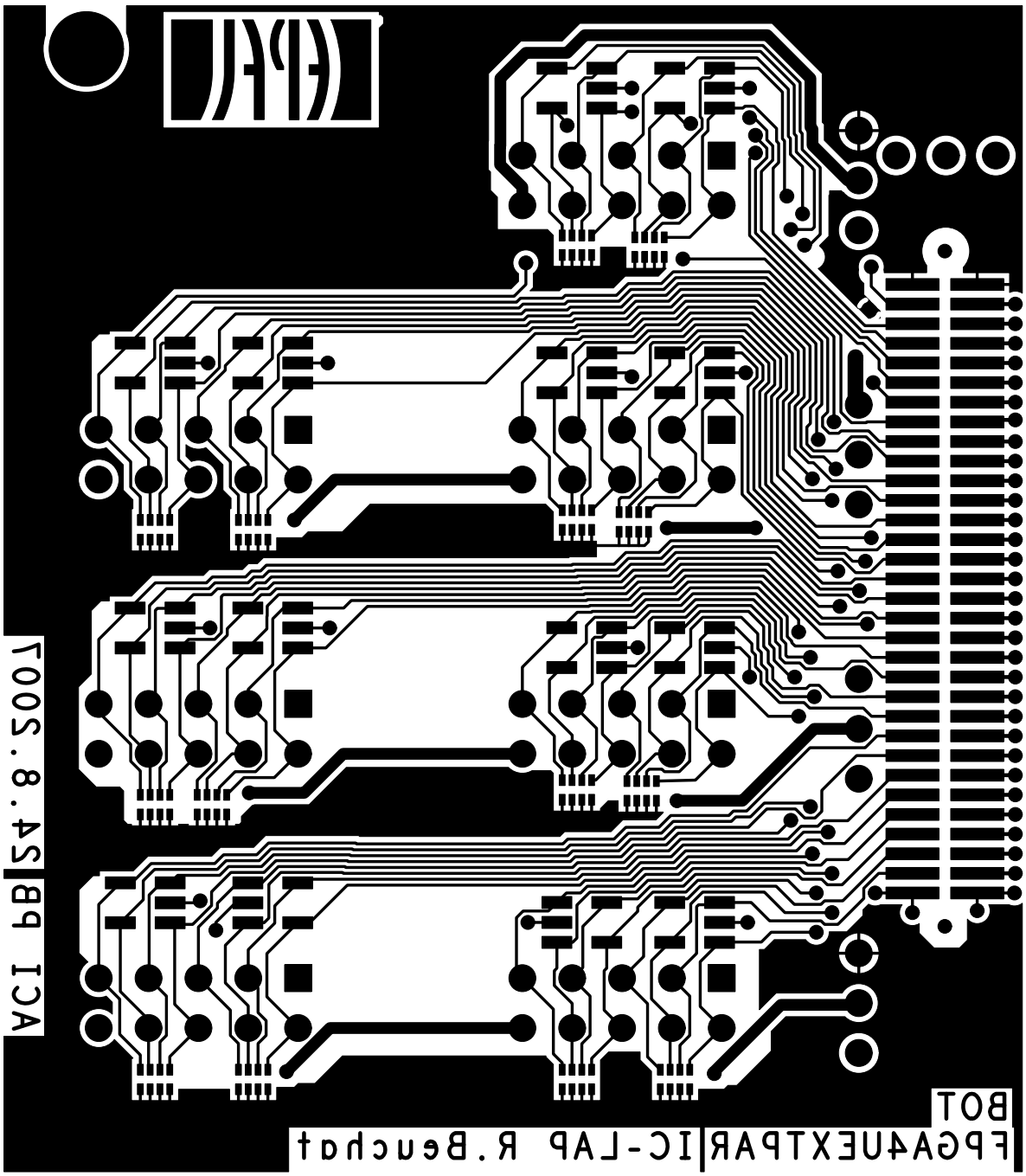


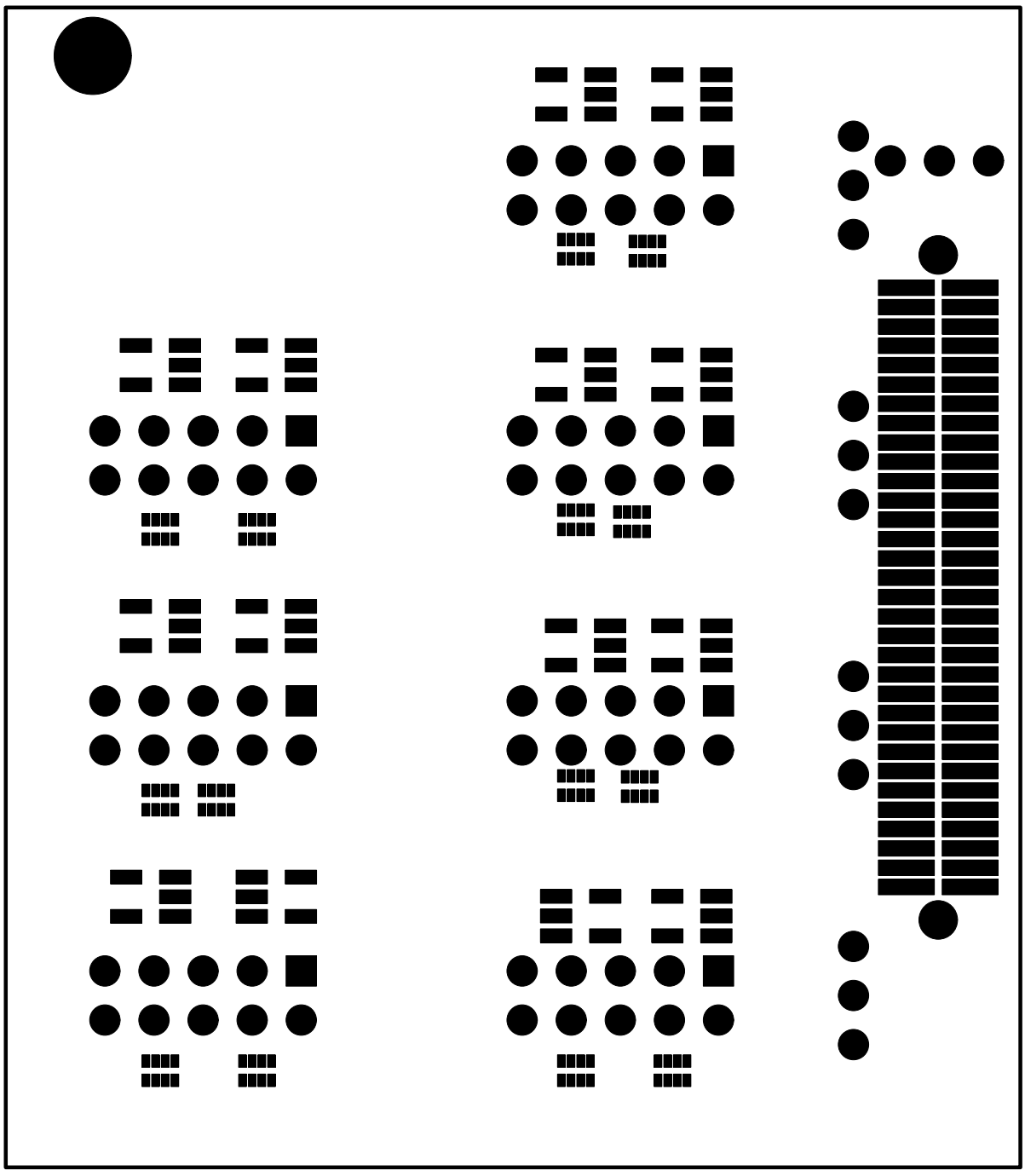
TITRE:FPGA4UEXTPAR	LABORATOIRE:IC-LAP	DATE:24.8.2007
	ENGINEER:R.Beuchat	EPFL-ACORT-PB

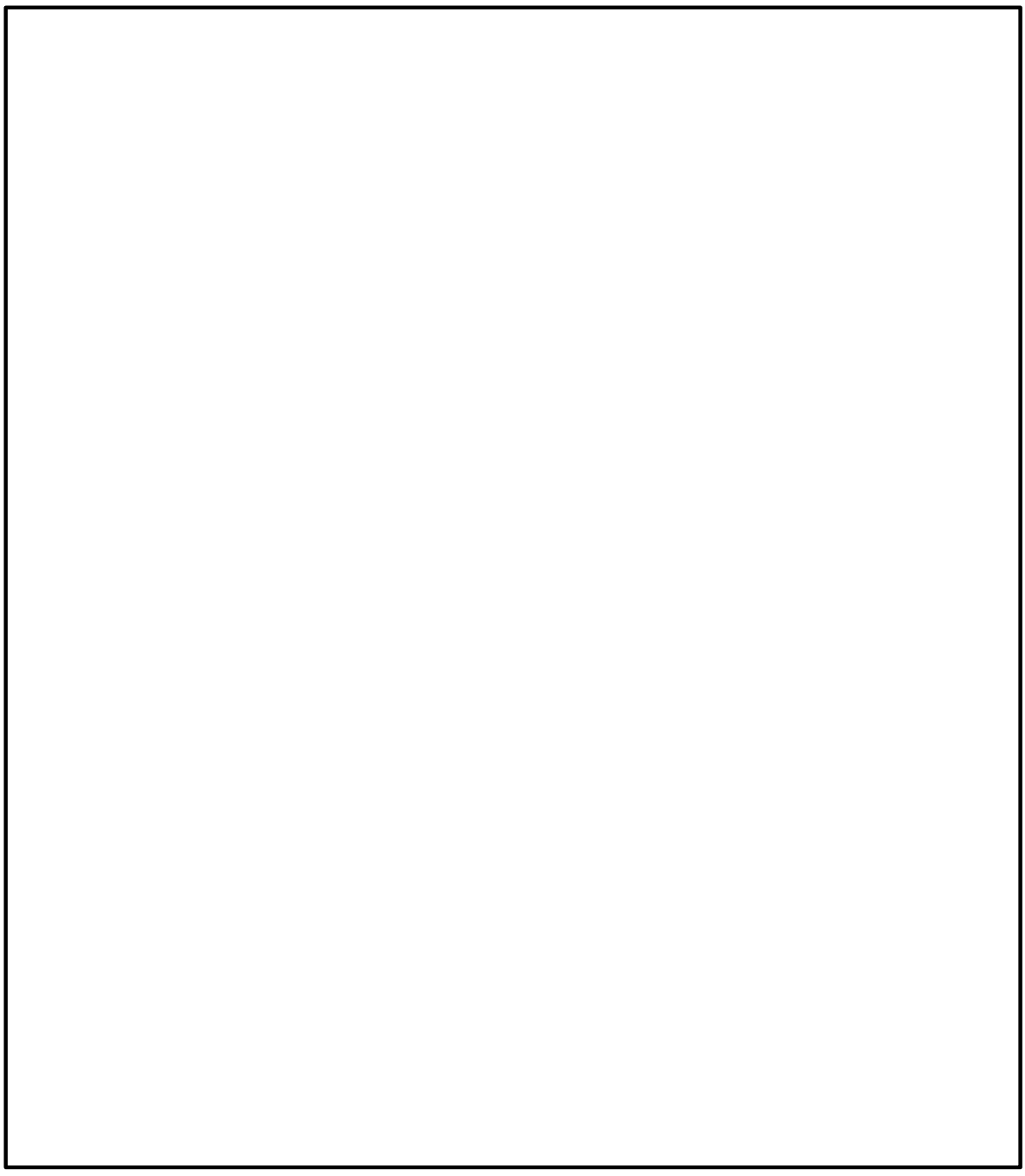
EPFL ACORT Wed 29.08.2007 11:32 Drawing name = FPGA4UEXTPAR Scale = 1.00 1.000 Inch =




FPGA4UEXTPAR
IC-LAP R.Beuchat
ACI PB
TOP
24.8.2007


FPGA4UEXTPAR IC-LAP R.Beuchat
BOT
ACI 4B 24.8.2007





Component Report FPGA4UEXTPAR

fpga4uextpar_gloss Wed Aug 29 11:33:11 MET DST 2007

Ref Des	Device Type	Value	Package Type	x	y	ang	Mir	Remark
D1	SP0504BAHTG	SP0504BAHTG	SOT23_5	27.000	41.500	0.000	YES	
D2	SP0504BAHTG	SP0504BAHTG	SOT23_5	33.000	41.500	0.000	YES	
D3	SP0504BAHTG	SP0504BAHTG	SOT23_5	27.000	28.000	0.000	YES	
D4	SP0504BAHTG	SP0504BAHTG	SOT23_5	33.000	28.000	0.000	YES	
D5	SP0504BAHTG	SP0504BAHTG	SOT23_5	26.500	14.000	0.000	YES	
D6	SP0504BAHTG	SP0504BAHTG	SOT23_5	33.000	14.000	180.000	YES	
D7	SP0504BAHTG	SP0504BAHTG	SOT23_5	48.750	13.000	180.000	YES	
D8	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	13.000	0.000	YES	
D9	SP0504BAHTG	SP0504BAHTG	SOT23_5	49.000	27.000	0.000	YES	
D10	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	27.000	0.000	YES	
D11	SP0504BAHTG	SP0504BAHTG	SOT23_5	48.500	41.000	0.000	YES	
D12	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	41.000	0.000	YES	
D13	SP0504BAHTG	SP0504BAHTG	SOT23_5	48.500	55.500	0.000	YES	
D14	SP0504BAHTG	SP0504BAHTG	SOT23_5	54.500	55.500	0.000	YES	
J1	CO64		MO64MSMD_1MM	67.250	30.000	90.000	YES	
J10	CO10		CPMD10	55.880	10.160	180.000	NO	
J11	CO10		CPMD10	34.290	10.160	180.000	NO	
J12	CO10		CPMD10	55.880	24.130	180.000	NO	
J13	CO10		CPMD10	34.290	24.130	180.000	NO	
J14	CO10		CPMD10	55.880	38.100	180.000	NO	
J15	CO10		CPMD10	34.290	38.100	180.000	NO	
J16	CO10		CPMD10	55.880	52.070	180.000	NO	
J17	CO3		JUMP3	64.770	54.610	180.000	YES	
RN1	RN0805	1K	RN4_0804	27.000	33.000	90.000	YES	
RN2	RN0805	1K	RN4_0804	32.000	33.000	90.000	YES	
RN3	RN0805	1K	RN4_0804	27.000	19.000	90.000	YES	
RN4	RN0805	1K	RN4_0804	29.900	19.000	90.000	YES	
RN5	RN0805	1K	RN4_0804	27.000	5.000	90.000	YES	
RN6	RN0805	1K	RN4_0804	32.000	5.000	90.000	YES	
RN7	RN0805	1K	RN4_0804	48.500	5.000	90.000	YES	
RN8	RN0805	1K	RN4_0804	53.500	5.000	90.000	YES	
RN9	RN0805	1K	RN4_0804	48.500	19.750	90.000	YES	
RN10	RN0805	1K	RN4_0804	51.800	19.700	90.000	YES	
RN11	RN0805	1K	RN4_0804	48.500	33.500	90.000	YES	
RN12	RN0805	1K	RN4_0804	51.400	33.400	90.000	YES	
RN13	RN0805	1K	RN4_0804	48.500	47.500	90.000	YES	
RN14	RN0805	1K	RN4_0804	52.200	47.400	90.000	YES	
V1	VIS_METAL		VIS2	23.500	57.500	0.000	NO	
W1	JUMP3		JUMP3	65.405	6.350	90.000	NO	
W2	JUMP3		JUMP3	65.405	20.320	90.000	NO	
W3	JUMP3		JUMP3	65.405	34.290	90.000	NO	
W4	JUMP3		JUMP3	65.405	48.260	90.000	NO	

Total Component count 42

BOM Report FPGA4UEXTPAR

fpga4uextpar_gloss — Wed Aug 29 11:33:11 MET DST 2007

Device	Package	Value	Nb	Reference Designators					Remark
CO10-CPMD10	CPMD10		7	J10	J11	J12	J13	J14	
				J15	J16				
CO3-JUMP3	JUMP3		1	J17					
CO64-MO64MSMD_1MM	MO64MSMD_1MM		1	J1					
JUMP3-1	JUMP3		4	W1	W2	W3	W4		
RN0805-1-1K	RN4_0804	1K	14	RN1	RN2	RN3	RN4	RN5	
				RN6	RN7	RN8	RN9	RN10	
				RN11	RN12	RN13	RN14		
SP0504BAHTG-SP0504BA	SOT23_5	SP0504BAHTG	14	D1	D2	D3	D4	D5	
				D6	D7	D8	D9	D10	
				D11	D12	D13	D14		
VIS_METAL-M2	VIS2		1	V1					

Total Component count 42

NC Pins Report FPGA4UEXTPAR

fpga4uextpar_gloss Wed Aug 29 11:33:12 MET DST 2007

Ref Des	Device	Nb	Not Connected Pins	Remark
V1	VIS_METAL-M2	1	1	
	Total count 1			

Power Pins Report FPGA4UEXTPAR

fpga4uextpar_gloss Wed Aug 29 11:33:13 MET DST 2007

Ref Des	Device	Name	Power Pins	Remark
D1	SP0504BAHTG-SP0504BA	GND	2	
D2	SP0504BAHTG-SP0504BA	GND	2	
D3	SP0504BAHTG-SP0504BA	GND	2	
D4	SP0504BAHTG-SP0504BA	GND	2	
D5	SP0504BAHTG-SP0504BA	GND	2	
D6	SP0504BAHTG-SP0504BA	GND	2	
D7	SP0504BAHTG-SP0504BA	GND	2	
D8	SP0504BAHTG-SP0504BA	GND	2	
D9	SP0504BAHTG-SP0504BA	GND	2	
D10	SP0504BAHTG-SP0504BA	GND	2	
D11	SP0504BAHTG-SP0504BA	GND	2	
D12	SP0504BAHTG-SP0504BA	GND	2	
D13	SP0504BAHTG-SP0504BA	GND	2	
D14	SP0504BAHTG-SP0504BA	GND	2	
J1	CO64-MO64MSMD_1MM	GND	13 14 63 64	
		VCC	1 2	
J10	CO10-CPMD10	GND	1	
J11	CO10-CPMD10	GND	1	
J12	CO10-CPMD10	GND	1	
J13	CO10-CPMD10	GND	1	
J14	CO10-CPMD10	GND	1	
J15	CO10-CPMD10	GND	1	
J16	CO10-CPMD10	GND	1	
J17	CO3-JUMP3	GND	1	
RN1	RN0805-1-1K	VCC	2 4 6 8	
RN2	RN0805-1-1K	VCC	2 4 6 8	
RN3	RN0805-1-1K	VCC	2 4 6 8	
RN4	RN0805-1-1K	VCC	2 4 6 8	
RN5	RN0805-1-1K	VCC	2 4 6 8	
RN6	RN0805-1-1K	VCC	2 4 6 8	
RN7	RN0805-1-1K	VCC	2 4 6 8	
RN8	RN0805-1-1K	VCC	2 4 6 8	
RN9	RN0805-1-1K	VCC	2 4 6 8	
RN10	RN0805-1-1K	VCC	2 4 6 8	
RN11	RN0805-1-1K	VCC	2 4 6 8	
RN12	RN0805-1-1K	VCC	2 4 6 8	
RN13	RN0805-1-1K	VCC	2 4 6 8	
RN14	RN0805-1-1K	VCC	2 4 6 8	
W1	JUMP3-1	GND	1	
		VCC	3	
W2	JUMP3-1	GND	1	
		VCC	3	
W3	JUMP3-1	GND	1	
		VCC	3	
W4	JUMP3-1	GND	1	
		VCC	3	
	Total count 41			

Single Node Nets Report FPGA4UEXTPAR

fpga4uextpar_gloss Wed Aug 29 11:33:13 MET DST 2007

Netname	Node	Device	Remark

Total Nets count 0